TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT,
AND GENERAL SUPPORT MAINTENANCE
(INCLUDING REPAIR PARTS AND SPECIAL TOOLS LISTS)
FOR
DATA ANALYZER DA-404
(STELMA MODEL DA-404)

HEADQUARTERS, DEPARTMENT OF THE ARMY

15 OCTOBER 1980

WARNING

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

CAUTION

Do not make more than one input connection at a time. Use only the appropriate input jack, and leave the other input jack unconnected.

NOTE

Do not destroy or discard the packing case. It can be used when reshipping the unit to the manufacturer or repair facility in case of equipment damage or malfunction.

TECHNICAL MANUAL

No. 11-6625-2815-14&P

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HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, DC, *15 October 1980*

**OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT,
AND GENERAL SUPPORT MAINTENANCE
(INCLUDING REPAIR PARTS AND SPECIAL TOOLS LIST)
FOR
DATA ANALYZER DA-404
(STELMA MODEL DA-4)
Current as of 30 May 1980**

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS
      You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blanks Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703.
      In either case, a reply will be furnished direct to you.

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LIST OF TABLES

This manual is an authentication of the manufacturer's commercial literature which, through usage, has been found to cover the data required to operate and maintain this equipment. Since the manual has not been prepared in accordance with military specifications and AR 310-3, the format has not been structured to consider level of maintenance.

SECTION O

INSTRUCTION

0-1. SCOPE

This manual describes Data Analyzer, Stelma Model DA-404, and provides instructions for operation, maintenance, and performance testing. Throughout this manual, the DA-404 is referred to as Data Analyzer.

0-2. INDEXES OF PUBLICATIONS

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.
b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

0-3. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System.
b. Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 735-11-2/NAVSUPINST 4440.127E/AFR 400-54/MCO 4430.3E and DSAR 4140.55.
*c. Discrepancy in Shipment Repo*rt *(DISREP) (SF 361). Fill* out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C and DLAR 4500.15.

0-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

If your Data Analyzer, Stelma Model DA-404, needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Tell us why a procedure is hard to perform. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications and Electronics Materiel Readiness Command, ATIN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703. Well send you a reply.

0-5. ADMINISTRATIVE STORAGE

Administrative storage of equipment issued to and used by Army activities shall be in accordance with paragraph 5-5.

0-6. DESTRUCTION OF ARMY ELECTRONICS MATERIEL

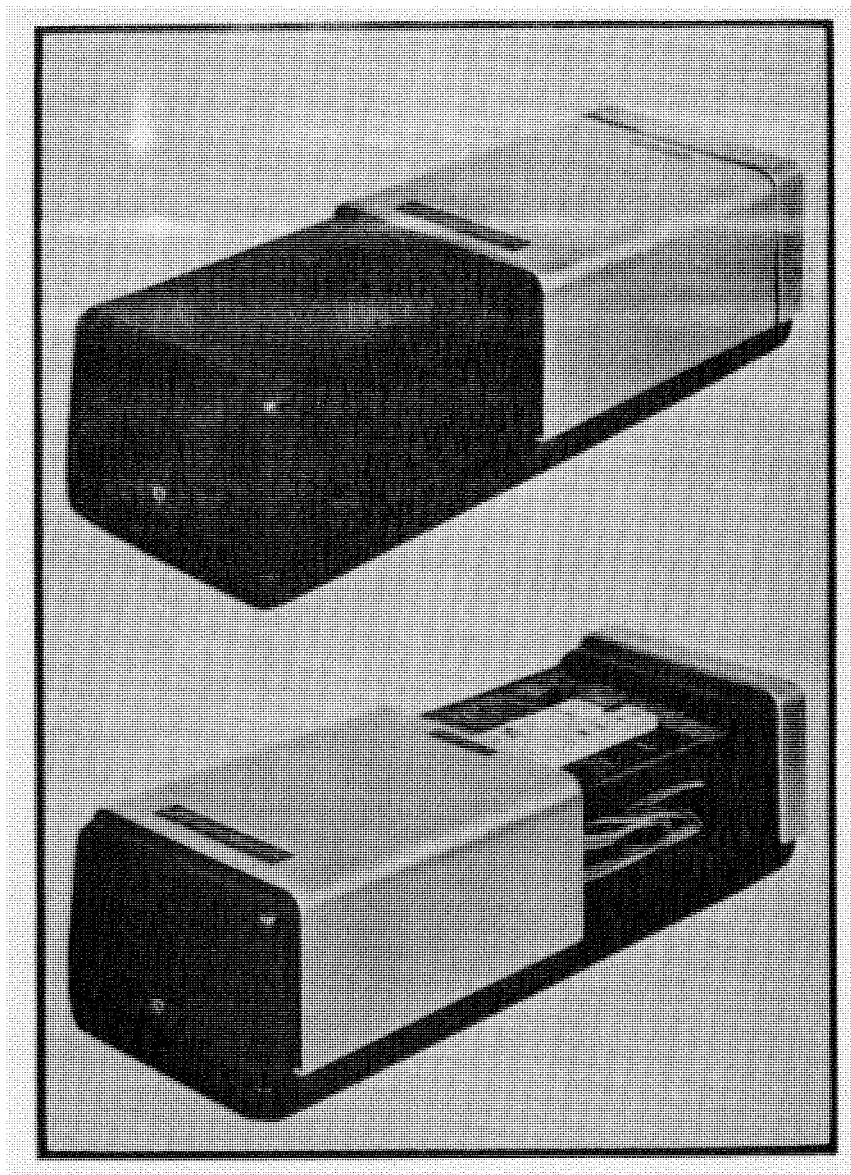Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Figure 1-1. Data Analyzer, Model DA-404.

SECTION I

INTRODUCTION

1-1. DATA ANALYZER

a. Data Products' Data Analyzer DA-404 (fig. 1-1) is a compact, portable, ac/battery operated test set that measures and indicates the type and magnitude of distortion present in all characters of start stop (asynchronous) data/telegraph signals; the monitored signal may be 5-level, and either 7-level or 8-level code (strap selectable)-using low-level polar : 3 to :25 volts, high-level polar (10 to 30ma), or neutral (20 or 60ma) inputs. The unit also indicates the presence of detected parity errors in 7- or 8-level coded data signals.

b. Measurements may be made at any one of four customer specified, standard baud-rates, ranging from 37.5 to 300 bauds. While measuring end or bias distortion (Marking or Spacing), the Data Analyzer also simultaneously indicates total peak distortion present in the signal. Used with an associated test pattern generator (such as Pattern Generator, Data Products' Model PG-404), the Data Analyzer provides a comprehensive field capability for testing and evaluating the performance of data/telegraph systems and equipment.

1-2. DESCRIPTION

a. Basically, the Data Analyzer comprises four principal sections: distortion measurement circuit, parity error detector, input circuits, and power supply.

(*1*) *Distortion Measurement Circuits.* The Data Analyzer measures both of the following types of asynchronous signal degradations:

    (a) Average bias and total peak distortion.

    (*b*) Average end and total peak distortion.

NOTE

Peak distortion readouts can be either bias or end distortion, whichever is higher.

(*2*) *Bias or end distortion,* as well as peak distortion readouts are simultaneously displayed on a solid-state meter, using light emitting diodes (LEDs) mounted behind a smoked plexiglass panel. The panel is marked in graduations of percent distortion, from 0 to 50, in 3-1/3 percent increments. When measuring bias or end distortion, the sense (Marking or Spacing) of the detected distortion is displayed by two LED indicators. Peak distortion measurement may be reset by depressing a front-panel pushbutton.

(*3*) *Parity Error Detector.* The unit detects and indicates odd- or even- (strap selectable) parity errors in 7-level or 8-level coded signals. The parity error indicator may be reset, by means of the same pushbutton that resets the peak distortion indicator.

(*4*) *Input Circuits.* The Data Analyzer accommodates three types of data/telegraph input signal:

    (a) Low-*l*evel logic (t 3 to t 25 volts) that, by means of a front-panel polarity-reversing (POLARITY REV) switch, may be made to conform with EIA Standard RS-232B (negative Mark) or MIL-MTD-188B (positive Mark).

    (*b*) High-level neutral loops (20 or 6(mn).

NOTE

Through the use of the POLARITY REV switch, neutral input loops can be wired with either positive or negative jack tips.

    (c) High-level polar loops (10 to 30ma).

(*5*) *Power Supply.* Data Analyzer d operating voltages are supplied by an inverter circuit powered by: (1) an internal, rechargeable 5 volt battery (during battery operation); or (2) a full-wave power supply (during ac operation). Recharging current *is* supplied to the battery when the ac line cord is connected to a 115-volt or 230-volt (strap selectable), 60Hz power source. Battery recharging occurs when the front-panel PWR switch is off (heavy charge), or when the equipment is operating (trickle charge). The battery condition may be checked by means of a front-panel pushbutton and indicator lamp.

b. As shown in figure 1-1, the Data Analyzer is contained in a 2-piece, molded plastic carrying case provided with a fold-away handle. All operating controls and indicators, located on the top panel, are protected by a sliding aluminum cover; when open, the sliding cover permits access to the ac line cord storage compartment in the side of the unit. Input signal connections are made at jacks on the front panel; ac power and loop fuses are recessed in the bottom of the unit.

c. Al Data Analyzer electronics are solid-state--including integrated circuits (ICs) and, except for the power transformer and batteries, are constructed on three printed circuit (PC) cards (Assemblies Al, A2, and A3). For access to internal components for maintenance and repair, as required, the upper portion of the carrying case may easily be removed.

Table 1-1. Technical Specifications

Item	Description
INPUT SIGNAL:	
Speeds	Any standard four customer-specified (strap selectable) rates from 37.5 to 300 bauds.
Mode	Start-stop (asynchronous).
Format	5-level, and either 7-level or 8-level code.
Levels	20/60ma neutral; 10 to 30ma (high-level) polar; t 3- to + 25-volt (low-level) polar, RS-232B/MIL-STD-188B
compatible.	
Impedance	100 ohms, 60ma loop; 300 ohms, 20ma loop; 25,000 ohms, low-level input.
Polarity	Selectable by front-panel switch.
DISTORTION	
MEASUREMENT:	
Types	Bias or end distortion, and simultaneous peak distortion. (Peak distortion readout may be either bias or end peak, whichever is higher.)
Range	0 to 50 per cent, in 3-1/3 percent increments.
Accuracy	3-113 percent.
PARITY	Odd or even parity (strap selectable) for 7- or 8-level codes.
MEASUREMENT	
PARITY ERROR	Lamp indicates parity error (odd or even, strap selectable); indicator lamp is reset by front-panel pushbutton.
OPERATING MODES	Ac or battery.
BATTERY MODE OPERATING TIME	More than 12 hours of continuous operation, with fully charged battery.
BATTERY CHARGING TIME	16 hours (approximate) from full-discharge to full-charge condition, with power OFF; unit may be operated while battery is being recharged (trickle charge).
POWER	
REQUIREMENTS:	
Ac	115 or 230 volts (strap selectable), 60 Hz.
Battery	6 volts, rechargeable NICD.
DIMENSIONS (inches)	3-13/16 wide, 11-112 high, 3-5/8 deep.
WEIGHT(pounds)	3-1/2.

1-3. PREPARATION FOR USE

a. Unpacking.

(1) When shipped from the factory, the Data Analyzer has all customer-specified wiring options installed so that it may be placed into operation immediately after it has been unpacked.

(2) Remove the Data Analyzer from its packing case, and carefully check for damage that may have occurred during shipment. Immediately notify the carrier and/or the manufacturer of any damage to the equipment.

NOTE

Do not destroy or discard the packing case. It can be used when reshipping the unit to the manufacturer or repair facility in case of equipment damage or malfunction.

b. Electrical Connections.

(1) Use of the Data Analyzer with low-level, high-level polar, or neutral loop circuits requires that proper external connections be made to the front-panel jacks. Particular applications may require that certain customer-specified factory wired strapping connections be changed; the Data Analyzer contains strapping terminals for such alternate configurations, to satisfy requirements of different system applications and uses. Refer to paragraph 4-6 for a description of the various strapping options.

(2) Input jacks for high-level (neutral or polar) and low-level (polar) signals are located on the unit's front panel. The input jacks to be used depend on the type of circuit being tested.

(a) Use a Western Electric plug Type 347 (or equivalent) for connections to the HI LEVEL LOOP jack; once this connection is made, select either high-level polar or neutral loop monitoring by means of the push buttons at the unit's top panel.

(b) Use a Pomona type MDP dual banana plug (or equivalent) for connections to the LOW LEVEL jacks.

CAUTION

Do not make more than one input connection at a time. Use only the appropriate input jack, and leave the other input jack unconnected.
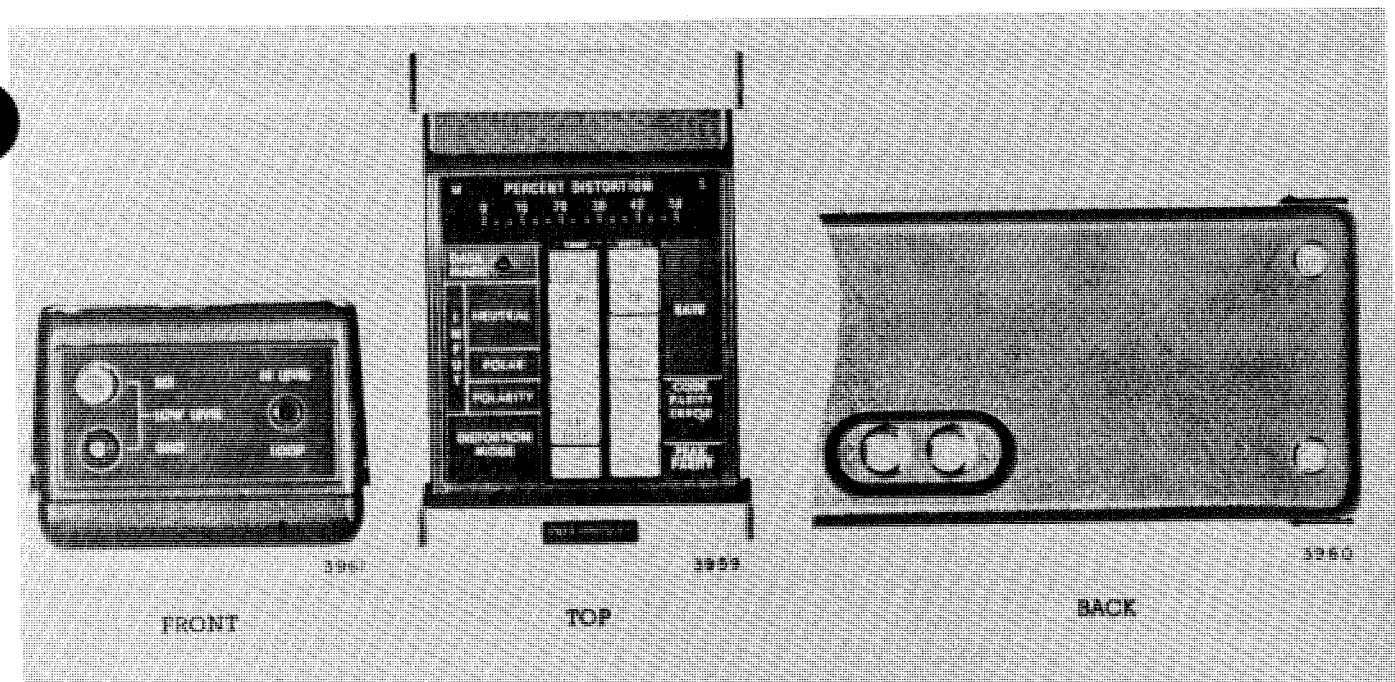
Figure 2-1. Data Analyzer-front, top, back views.

1-3

SECTION II

OPERATION

2-1. OPERATING DATA ANALYZER
All controls and indicators used during normal operation of the Data Analyzer are located on the top panel, and

input signal connections are made at the front panel (fig. 2-1). Fuses are located on the bottom of the unit.

Table 2-1. Controls, Indicators, Jacks, Fuses

Control, Indicator, Jack or Fuse	Function
DATA MARK indicator lamp	Lights when Mark signal is received.
PWR switch	When pressed, applies power to Distortion Analyzer.
INPUT switches	
NEUTRAL	Condition Data Analyzer to monitor:
20MA	20ma neutral loop inputs.
60MA	60ma neutral loop inputs.
POLAR	Conditions Data Analyzer to monitor high-level (10 to 30ma) or low-level (+ 3 to x 25 volts) polar input. (High- or low-level determined by front-panel jack connection.)
POLARITY REV switch	Up (i.e., not pressed) position conditions Data Analyzer for positive Mark polar inputs and positive tip neutral inputs. When pressed, conditions Data Analyzer for negative Mark polar inputs and negative tip neutral inputs.
DISTORTION MODE switches	Select simultaneous:
BIAS PEAK	Average bias distortion and total peak distortion (bias or end, whichever is higher) readouts for display on PERCENT DISTORTION indicator.
END PEAK	Average end distortion and total peak distortion (bias or end, whichever is higher) readouts for display on PERCENT DISTORTION indicator.
RATE switches (four)	Each selects specified baud-rate, according to signal being monitored.
CODE switches:	Condition Data Analyzer to monitor:
5 LEV	5-level code inputs.
8 LEV (or 7 LEV)	8-level or 7-level code inputs (whichever is established by strap option).
PARITY ERROR indicator lamp	Performs two functions: a. Lights to indicate parity error in 8-level or 7-level character; is extinguished when RESET switch is pressed and released. b. Lights brightly, when RESET switch is pressed and held, if battery has at least 0.5 operating hour remaining, thus indicating condition of internal battery.
RESET PEAK switch PARITY	Performs three functions: a. Press-and-release resets peak distortion readout on PERCENT DISTORTION indicator; press-and-hold displays average distortion only. b. Press-and-release, when PARITY ERROR lamp is lighted, extinguishes lamp. c. Press-and-hold, in conjunction with PARITY ERROR lamp, indicates condition of internal battery.
PERCENT DISTORTION indicator	Solid-state meter containing 16 LEDs, any two of which simultaneously indicate average and total peak distortion. Readouts are in increments of 3-1/3 per cent, from 0 to 50.
M indicator lamp (part of PERCENT DISTORTION indicator)	Lights to indicate average Marking distortion condition; used with DISTORTION MODE switches to indicate average Marking bias or average Marking end distortion.
S indicator lamp (part of PERCENT DISTORTION indicator)	Lights to indicate average Spacing distortion condition; used with DISTORTION MODE switches to indicate average Spacing bias or average Spacing end distortion.
LOW LEVEL (SIG and GND) jacks	Provide input connections for low-level input signal.
HI LEVEL LOOP jack	Provides input connection for high-level polar (10 to 30ma) or neutral loop (20 or 60ma) input signals.
AC fuse	Fuses ac power line.
LP fuse	Fuses high-level (polar and neutral loop) input signal line.

2-2. PRELIMINARY SETUP

The general procedure for setting up the Data Analyzer before operating the unit is described below:

a. Make certain that the correct internal strapping connections have been made for the given application.

b. Determine whether the mode of operation will be ac or battery.

(1) For the ac mode, connect the ac line cord to a 115- or 230-volt (as required), 60-Hz power source.

(2) For battery mode, check the condition of the internal battery by pressing the RESET switch and observing the PARITY ERROR indicator lamp. Use the chart below as a guide to determine whether the battery's condition will permit battery operation.

Indicator Lamp Intensity Level	Battery Condition
Dark (lamp does not light).	Completely discharged. Output voltage too low to operate unit.
Dim	Almost fully discharged. Battery should be recharged.
Bright	Output voltage can operate unit for at least 0.5 hour.

2-3. OPERATING PROCEDURES

After performing the preliminary setup, use the procedure outlined below as a guide for operating the Data Analyzer.

a. Select the type of loop circuit being monitored by pressing the appropriate INPUT switch. Three selections are available: NEUTRAL-20MA, NEUTRAL 60MA, or POLAR. The POLAR switch must be pressed for either high-level or low-level polar loop circuits.

b. If the input Marking signal is negative polar or negative tip neutral, press the INPUT-POLARITY REV switch. If the input Marking signal is positive polar or positive tip neutral, this switch need not be operated.

c. Make the proper input connections on the front panel (para 1-3b).

d. Select the baud-rate of the input signal by pressing the appropriate RATE switch.

e. Select the type of signal being monitored by pressing the appropriate CODE switch. Two selections are available: 5 LEV, and 8 LEV (or 7 LEV).

f. Determine the type of distortion analysis to be made by pressing either of two DISTORTION MODE switches:

(1) Selection of the BIAS/PEAK switch will provide indications of average percent bias distortion.

(2) Selection of the END/PEAK switch will provide indications of average percent end distortion.

NOTE

In both cases, total peak distortion indications (either bias or end, whichever is higher) are also provided at the same time.

g. Turn on the Data Analyzer by pressing the PWR switch. Check to see that the DATA MARK indicator lamp:

(1) Blinks intermittently if a data pattern is being received.

(2) Remains ON if a steady Mark input is being received.

(3) Remains OFF if a steady Space input is being received.

h. Press RESET switch.

2-4. INTERPRETING INDICATIONS

After the operating procedures described in paragraph 2-3 have been performed, percent and type distortion and parity-error incidence (7- or 8-level only) may be monitored.

a. Percent distortion presentation is available on the PERCENT DISTORTION display readout.

(1) If the DATA MARK indicator is not blinking (steady Mark or Space on the line), press the RESET switch; the PERCENT DISTORTION readout should indicate zero. If the DATA MARK indicator is blinking (data pattern being received) and distortion is present in the input signal, the PERCENT DISTORTION readout will provide one or two indications via the lighted red LEDs under the 0 to 50 PERCENT DISTORTION display scale (if two LED indications are presented, the lower one defines average distortion, and the higher defines peak distortion).

(2) Each graduation of the PERCENT DISTORTION scale represents 3-113 percent, + 1-213 percent. Thus, for example, a display as shown in figure 2-2 would indicate an average Marking bias (or end) distortion of 10 percent with a total peak distortion (bias or end) of 27 percent.
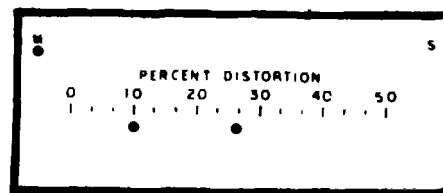
TYPICAL PERCENT DISTORTION READOUT

EL2PQO03

Figure 2-2. Typical Percent Distortion Readout.

b. Type of distortion present in the monitored signal is defined by the DISTORTION MODE switch that is pressed (i. e., bias distortion or end distortion).

(1) To further define the type of bias or end distortion present, two LED indicator lamps (M and S) are provided in the upper left-hand and right-hand corners, respectively, of the PERCENT DISTORTION display (fig. 2-2). If the BIAS/PEAK switch is pressed

and the M indicator lamp is lighted, the PERCENT DISTORTION readouts represent the amount of average Marking bias and total peak distortion. If the END/PEAK switch is pressed and the M indicator lamp is lighted, the PERCENT DISTORTION readouts represent the average Marking end and total peak distortion. In either mode, the total peak distortion readout may be either bias or end, whichever is higher. A graphic representation of the different types of bias is shown in figure 2-3. Note that total peak distortion is the maximum excursion of any transition from nominal. For a complete analysis of the distortion present in the monitored signal, two readings should be made: one with the BIAS/PEAK switch pressed, and another with the END/PEAK switch pressed.

(2) Several peak distortion measurements should be made while analyzing a particular signal because one high peak reading may be only a random occurrence that does not represent the true peak distortion over a period of time. Peak-reading samplings are effected by means of the RESET switch. Each time the switch is pressed and released, the peak distortion indication will be erased and the new peak distortion indication will appear. If the data signal being monitored contains a constant or unchanging amount of distortion, the bias/end and peak readings will be identical; thus, only one red LED indication will appear on the PERCENT DISTORTION readout. This condition may be observed when monitoring the output of a test pattern generator but would be unusual when used on a live data circuit.

c. Parity errors occurring in 7- or 8-level code inputs light the PARITY ERROR indicator lamp. Once lighted, the indicator is not extinguished until the RESET switch is pressed and released.

2-5. OPERATIONAL CONDITION
After performing the operating procedures described in

paragraph 2-3, the Data Analyzer will be operational for the conditions established. With the unit connected to the particular type of data circuit for which it has been set up, the only change to be made on the operating Distortion Analyzer involves selection of either DISTORTION MODE switch (BIAS/PEAK or END/PEAK), and intermittent depression of the RESET pushbutton to reset the PARITY ERROR or percent peak distortion indications. During long periods of battery operation, occasionally check the condition of the battery, by means of the RESET switch and PARITY ERROR indicator, to insure optimum performance of the Data Analyzer.

2-6. BATTERY CHARGING PROCEDURE
When fully charged, the battery can supply power to operate the unit continuously for approximately 12 hours. If the battery discharges completely, it can be brought to full charge in approximately 16 hours by turning the unit OFF and connecting the line cord to an ac outlet. Operation of the unit can be immediately restored, even when the battery has been completely discharged, by inserting the ac line cord into a power outlet. During this operational time, the internal battery receives a trickle charge which helps restore the battery and maintain it in a charged condition. After long periods of battery operation, the battery should be recharged to restore it to a fully charged condition.

CAUTION
DO NOT permit extensive periods of discharge, or the life of the battery will be reduced. To preserve battery charge, always turn OFF power when the unit is not in use.
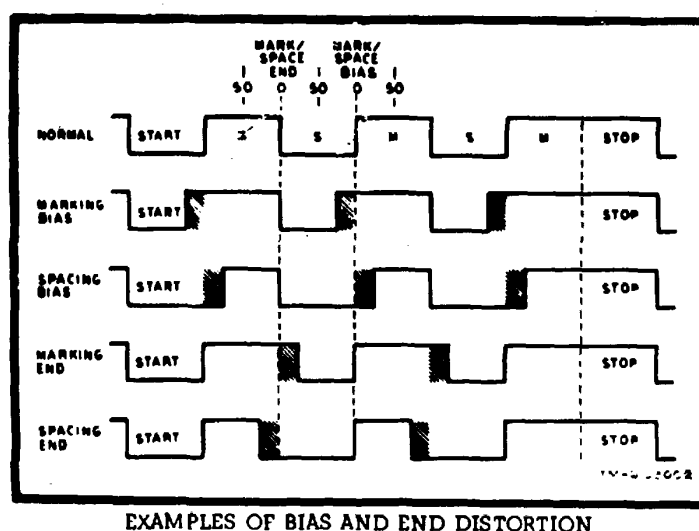
EXAMPLES OF BIAS AND END DISTORTION

EL2PQ004

Figure 2-3. Examples of Bias and End Distortion

SECTION III

PRINCIPLES OF OPERATION

3-1. OVERALL FUNCTIONAL DESCRIPTION

Data Analyzer operation is described in the following paragraphs on an overall basis, using a block diagram to illustrate interrelationships of major functional sections. Most Data Analyzer circuits are unrepairable IC modules, therefore, details are provided only for circuits that contain discrete components.

3-2. GENERAL

The Data Analyzer block diagram (fig. 3-1) shows major functional sections and principal control signals and data paths; power supply and switch control details are omitted for simplification Abbreviated signal names between functional blocks are the same as those shown on the schematic diagrams in the Maintenance section of this manual. As shown in the block diagram (fig. 2-4), the Data Analyzer comprises four major functional sections: input circuits, timing and control circuits, distortion measurement circuits, and output circuits.

a. The input circuit: provides the interface between the external polar or neutral input signal and the logic levels used in the Data Analyzer, and produces pulses that indicate the occurrence of every data-transition, and the beginning of a new character.

b. Pulses produced by the input circuits are used by the timing and control circuits to:

(1) Start the distortion count at the beginning of each character.

(2) Generate a time base for the selected baud-rate, which essentially divides each data-bit period into 30 increments (15 on either side of the center of a monitored data-bit). Each increment represents 3-1/3 percent distortion; thus, if data-bit transitions do not occur at the proper interval, the displacement from the normal transition point may be measured in increments of 3-1/3 percent distortion.

(3) Ensure that distortion measurements are made for the correct character-length (selected code) by disabling the timing and control circuit in the stop-Mark of the character; the circuit remains disabled until the beginning of the next character is detected.

c. The distortion measurement circuits:

(1) Count the total amount of distortion detected over a period of eight analyzed data-transitions, translate this total into an average count, and store the information (in BCD form) for subsequent display in the output circuits.

(2) Monitor the highest (peak) distortion count made, and store this information (in BCD form) for display in the output circuits.

d. The output circuits provide visual displays that indicate average and peak percent distortion, Marking or Spacing distortion, and parity error.

(1) Average and peak BCD values are multiplexed and decoded for simultaneous presentation on the PERCENT DISTORTION display.

(2) Using inputs from the timing and control and input circuits, the output circuit lights the M or S lamp to define the distortion present as Marking (lengthening of Mark-bits) or Spacing (lengthening of Space-bit), respectively.

(3) Parity-error indications are made on a character basis for 7- or 8-level codes; the parity error detector may be strapped for odd or even parity.

3-3. INPUT CIRCUITS, FUNCTIONAL DESCRIPTION

Primarily, the input circuits which comprise discrete transistor circuits, IC modules, and associated switches convert all inputs (low-level polar, high-level polar, and 20ma or 60ma neutral) into 0-to-5 volt Mark/Space (MIS) and Space/Mark (SIM) transitions used by the timing and control circuits. INPUT switches NEUTRAL-20MA, -60MA, and POLAR insure that all signals applied to the input circuit are of the same voltage amplitude; INPUT-POLARITY REV converts negative polar Mark (negative tip-neutral) inputs into positive Mark signals, within the input circuit. Thus, the input circuit operates the same way regardless of the type of polarity of the input signal. The input circuits produce four output signals: MI (Mark Indicator), High Mark, BP (Bias Pulse), and MSP (Mark/Space Pulse).

a. MI performs several functions:

(1) Low when a Mark input is present, it lights the DATA MARK indicator lamp.

(2) Applied with the High Mark signal through a DISTORTION MODE switch, it generates an MSC (Mark]Space Control) signal as described below.

(3) It functions in parity detector operations as described in paragraph *3-6d.*

b. The High Mark and MI signals applied via the DISTORTION MODE switches generate the MSC signal used in the Mark/Space indicator control circuit (para 2-6c) and the distortion measurement circuit (para 3-5).

(1) With BIAS/PEAK pressed, the MSC signal is high for Mark.

(2) With END/PEAK pressed, the MSC signal is high for Space.

c. BP pulses, generated at each M/S and S/M transi
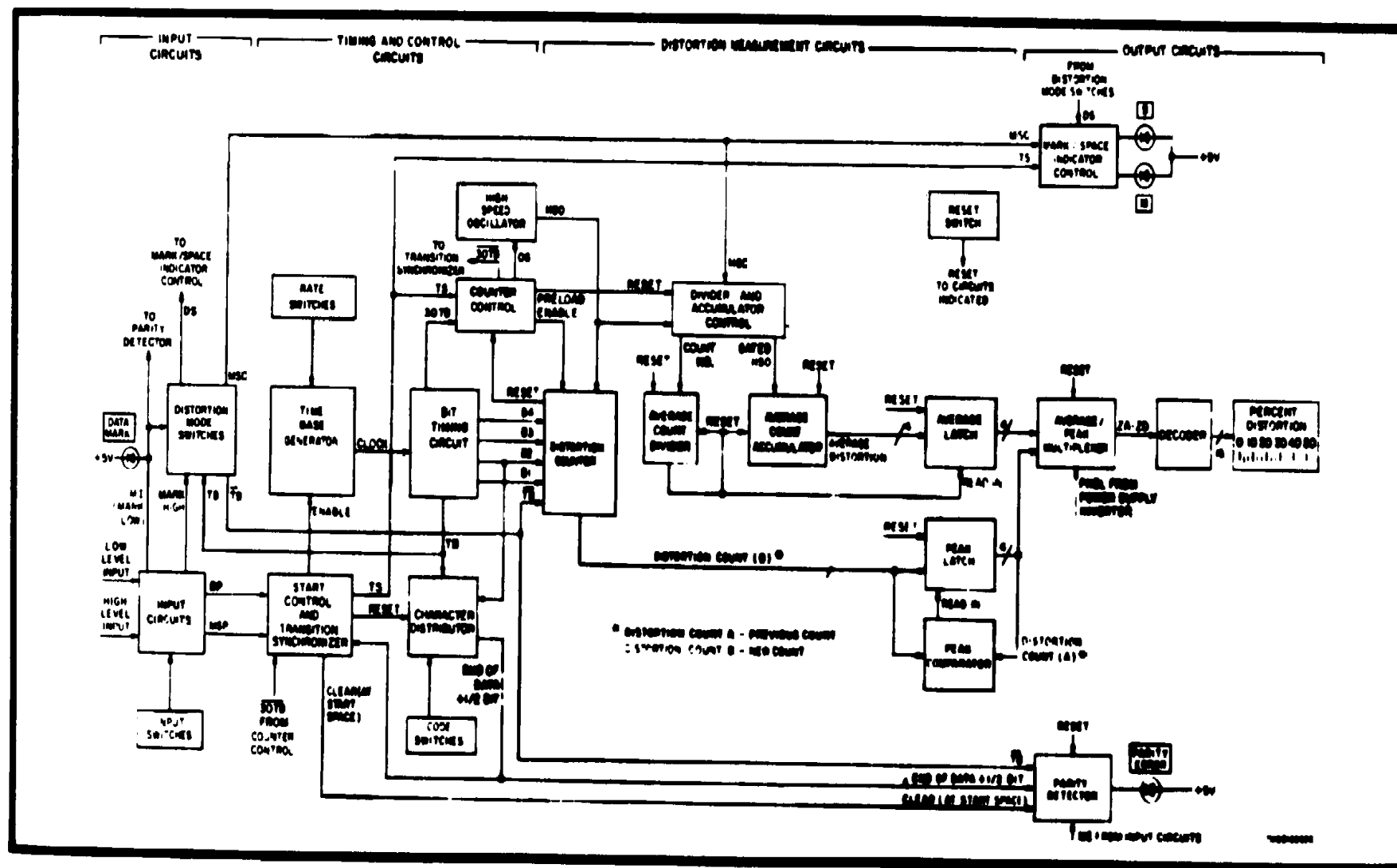
EL2PQ005

Figure 3-1. Data Analyzer, Block Diagram.

DATA ANALYZER, TIMING DIAGRAM

EL2PQ006

Figure 3-2. Data Analyzer, Timing Diagram.

3-4

against the previous one and thereby update its information so that the highest (peak) value distortion count is available for display. After counting to 15, the distortion counter applies a reset pulse to the counter control; thus the peak comparator enable signal goes low (logic 0) to disable peak comparator output until the next data-bit transition, whereupon the sequence is repeated.

(b) While the peak comparator enable signal is low, the divider and accumulator inhibit input is also low (since both are the complement of OG); the HSO and MSC inputs to the divider and accumulator control are thus prevented from being used to generate count number and gated HSO outputs for the average count divider and accumulator circuits, respectively. When the divider and accumulator inhibit input is high (from data-bit transition until distortion counter completes count), the divider and accumulator is permitted to output count number and gated HSO pulse. (For details, see description of the distortion measurement circuits (para 3-5)).

e. *High-Speed Oscillator.* Using an RC oscillator almost identical to that in the time base generator, the high-speed oscillator produces a clock frequency output (HSO) of approximately 70kHz. The oscillator is gated ON by an OG input from the counter control, which occurs at each transition of the monitored data input. The resultant outputs clock the distortion counter and average count accumulator in the distortion measurement circuits. When the distortion counter control reaches its maximum count (15), it resets the counter which, in turn, inhibits the OG signal and thereby disables the high-speed oscillator.

f. Character Distributor. Essentially a binary counter (with a NAND gate output) controlled by the 'selected top-panel CODE switch (5 LEV, and 8 LEV or
7 LEV), the character distributor insures that distortion measurements and parity error detection occur for the correct number of data-bits in the selected code (i.e., for the correct character-length).

(1) Initially turned ON at the beginning of a character (by a reset pulse from the start control and transition synchronizer), the character distributor counts data-bits, using TB as the counter input. By means of internal strapping and connections through the selected CODE switch, counter output is NANDed with TB and B2 to produce a pulse one-half a bit time after occurrence of the last data-bit in the character (one-half a bit into stop-Mark). Thus, for example, if a 5-level code is selected, the end-of-character pulse from the character distributor will occur 6-1/2 bit-times after the beginning of the start-Space bit (start-Space plus 5 data-bits, plus one-half bit). This output is reapplied to the start control and transition synchronizer, stopping operation of that circuit until the next M/S transition (beginning of new character) occurs, causing the entire cycle to be repeated.

(2) The end-of-character pulse also enables the parity detector to output a signal indicating whether or not a parity error was detected during that character.

3-5. DISTORTION, MEASUREMENT CIRCUITS, FUNCTIONAL DESCRIPTION

The Data Analyzer distortion measurement circuits comprise a distortion counter, divider and accumulator control, average count accumulator, average count divider, average latch, peak latch, and peak comparator, as shown in the block diagram (fig. 2-4). Using inputs from the timing and control circuits, the distortion measurement circuits produce two 4-bit binary outputs representing the average and peak distortion present in the monitored data-signal.

a. *Distortion Counter.* The distortion counter (four exclusive OR gates, four NAND gates, and a 4-stage counter) provides a binary output, the value of which represents the difference in time between the point when a data-bit transition should normally occur (per the selected baud-rate) and the point at which it actually occurs in a monitored data-bit. Inputs B1, B2, B3, B4, and TB establish the point at which the transition should normally occur.

(1) As shown in the timing diagram (fig. 2-5), zero distortion is present only when B1 through B4 are all high and TB is-low, or vice versa. For various values of distortion, B1 through B4 provide different logic-l/logic-0 combinations; TB is a logic 1 for the first half of the normal bit-time (Spacing bias or Marking end) and a logic 0 for the second half of the normal bit-time (Marking bias or Spacing end). Each resulting logic-0/logic-1 combination, representing B1 through B4 and TB, preloads the 4-stage counter with a particular binary value whenever a transition occurs in the monitored data-bit.

(2) When a data-bit transition is sensed, a preload enable pulse is applied from the counter control circuit to the distortion counter. Consequently, the 4-bit binary value established by the logic levels of B1 through B4 and TB, at the moment of transition, are preloaded into the 4-stage counter. A value of 15 (binary 1111), representing less than 1-2/3 per cent distortion, is the highest number that can be preloaded into, or counted by, the counter since it contains only four stages. Any other preloaded number indicates the presence of distortion. The quantity of distortion is equal to the difference in count between 15 and the preloaded number, with each count representing 3-1/3 percent distortion, + 1-2/3 percent. Thus, for example, a preloaded 12 indicates a difference of three counts, or 10, ± 1-2/3 percent distortion.

(3) The counter counts up from the preloaded value to 15 triggered by HSO clock pulses from the

high-speed oscillator. As described in paragraph 2-4e, the oscillator is enabled by an OG output from the counter control at the same time that the counter control provides the preload enable signal to the distortion counter. This count-up value (the complement of the preloaded value, with respect to 15), representing the percent distortion measured for a particular data-bit, is applied from the distortion counter to a peak latch and peak comparator as a 4-bit parallel binary number (count (B)). When the counter reaches the maximum count of 15, it outputs a reset pulse to the counter control, removing the preload enable and OG signals and thereby inhibiting the distortion counter.

(4) The above sequence is repeated on the next data-bit transition when the TS and 30TB inputs again cause the counter control to generate preload enable and OG outputs.

b. Divider and Accumulator Control. This circuit is enabled at each transition of a monitored data-bit, by application of HSO clock pulses from the high-speed oscillator; simultaneously, MSC inputs are provided from the input circuits via the selected DISTORTION MODE switch.

(1) Except that its amplitude is limited to 5 volts, the MSC input is a replica of the actual monitored data signal. The MSC signal may, however, assume one of two polarities, depending on which DISTORTION MODE switch is pressed. With BIAS/PEAK pressed, the Mark signal is positive; with END/PEAK pressed, the Space signal is positive. It is the positive portion of the MSC signal, in conjunction with the HSO input, that activates the divider and accumulator control. The selected MSC signal insures that bias distortion measurements will be made with respect to S*IM* transitions and that end distortion measurements will be made with respect to M/S transitions (both transitions being positive, as selected by the appropriate DISTORTION MODE switch).

(2) With MSC and HSO inputs present, the divider and accumulator control provides two outputs: count No., which is applied to the average count divider; and gated HSO, which is applied to the average count accumulator. These outputs are present until the distortion counter (para 3-5a) reaches its maximum count, at which time it outputs a reset pulse to the counter control circuit; the latter, in turn, applies an inhibit pulse to the divider and accumulator control. With this arrangement, the number of grated HSO pulses applied to the average count accumulator is the same as that applied to the distortion counter (with each pulse representing 3-1/2 percent, ± 1-2/3 per cent distortion). The count No. output to the average count accumulator represents the number of transitions (M/S or SIM) in the monitored data.

c. Average Count Accumulator. A 7-stage counter, this circuit stores the gated HSO count over a period of eight data-bits (controlled by the average count divider

described below). Each HSO count represents 3-1/3 + 1-2/3 percent distortion; therefore, the 7-stage counter stores the average distortion measured for a nominal character length.

(1) If maximum distortion (50 percent were present in each monitored data-bit, 15 HSO pulses would be loaded into the counter 8 times, for a total count of 120. Likewise, if only 3 percent distortion were present in each data-bit, 1 HSO pulse would be loaded into the counter 8 times, for a total count of 8. Other values of percent distortion in each data-bit would produce proportionate counts between 8 and 120.

(2) Only values between 8 and 120 have any significance; therefore, only the last four stages of the counter (decimal 8, 16, 32, and 64) are used. These outputs are equivalent to BCD values of 1, 2, 4, and 8, respectively. Sixteen possible logic-0/logic-1 combinations of these four outputs represent the average distortion measured for a particular character. Based on the previous examples: with 50 percent distortion, all four outputs would be logic 1 (decimal 15); with 3 percent distortion, the 8-count output would be logic 1 and the other three-outputs would be logic 0 (decimal 1).

(3) The four BCD output lines are applied to the average latch, which is controlled by the average count divider.

d. Average Count Divider. This circuit counts transitions of the monitored data-signal. After counting eight transitions, it resets itself, resets the average count accumulator, and provides a read-in signal to the average latch. In resetting itself and the average count accumulator, the average count divider effectively ends the period of one distortion measurement and allows the next period of measurement to begin.

(1) The selected measurement period (eight data transitions) represents a compromise that provides an average distortion count from a maximum of eight characters (one transition per character) to a minimum of two to three characters (three MIS or SIM transitions per 5-level character, or five M/S or SIM transitions per 8-level character). A longer period of integration would slow the response such that wide variations in distortion would be lost; only a long-term average, providing a less true representation, would thus be seen. If a shorter period were used, the distortion indication might change so rapidly that it would be useless.

(2) The read-in signal applied to the average latch allows the average distortion measurement at the input of the average latch to be transferred to the output side.

e. Average Latch. A storage device, the average latch receives four BCD inputs (from the average count accumulator) representing average distortion.

These inputs, constantly updated during the 8-transition measurement interval, are held in storage until the eighth data-transition occurs, at which time a read in signal is applied from the average count divider This signal enables the average latch to transfer the four stored logic bits to an average/peak multiplexer is the output circuit.

f. Peak Latch and Peak Comparator. The peak latch is identical with the average latch described in e above except that the peak latch operates in a slightly different way, under control of a peak comparator.

(1) The peak latch and peak comparator both receive four parallel logic inputs (count B) from the distortion counter; these inputs represent, in binary form, the distortion measured for a particular data-bit Count B (referred to as the new count) is compared by the peak comparator with the four logic bits, count A (referred to as the previous count), on the output side of the peak latch. This comparison takes place on each data-transition, when the counter control applies an enable signal to the peak comparator. If the previous count is less than the new count, the peak comparator provides a read-in signal to enable the peak latch t(transfer the new count to the average/peak multiplexer in the output circuit. With a new count appearing on the output side of the peak latch, both inputs to the peak comparator become equal and the read-in signal to the peak latch is disabled.

(2) The condition in (1) above is maintained until the peak latch input again exceeds the output, causing the sequence to be repeated. As a result, the peal (highest) distortion value is always presented to' the average/peak multiplexer.

3-6. OUTPUT CIRCUITS, FUNCTIONAL DESCRIPTION

Comprising an average/peak multiplexer, a decoder the PERCENT DISTORTION display, Mark/Space indicator

control, and parity detector, the output circuits provide the visual display that indicates: average and peak distortion; type (Marking or Spacing) of distortion; and parity errors in 7- or 8-level codes.

a. Average/Peak Multiplexer. The average/peak multiplexer (essentially, four pairs of AND gates, each pair driving an inverter output through a NOR gate) combines detected average and peak distortion, on a time-sharing basis, for simultaneous presentation on the PERCENT DISTORTION display. Four identical circuits are required, because the average and peak torsion outputs from the respective latching circuits are each represented by four binary logic bits.

(1) One AND gate of each pair receives a logic input from the average latch; the other AND gate, a logic input from the peak latch. However, only one AND gate in each of the four pairs is enabled at one time, by a 50kHz Peak Blanking (PKBL) pulse from a free-running multi-vibrator in the power supply inverter (para 3-8).

(2) Resultant output from the multiplexer (Za-Zd), a rapid alternation of four binary logic bits representing average and then peak distortion, is applied to a decoder.

b. Decorder. The decoder is basically a 4-by-16 matrix that converts the four alternating, binary coded, average/peak bits into a decimal output on 16 lines. The lines are connected to the 16 LEDs that produce the PERCENT DISTORTION display. Because of the rapid alternation of the average and peak distortion inputs, the displays appear to be simultaneous, but they are actually being turned ON and OFF at a 50kHZ rate. The chart below lists the 16 possible logic inputs and the resultant percent distortion display.

Z_D (8)	Z_C (4)	Z_B (2)	Z_A (1)	PERCENT* DISTORTION ($\pm$1-213)	Z_D (8)	Z_C (4)	Z_B (2)	Z_A (1)	PERCENT*. DISTORTION (+ 1-2/3)
0	0	0	0	0	1	0	0	0	26-213
0	0	0	1	3-113	1	0	0	1	30
0	0	1	0	6-2/3	1	0	1	0	33-1/3
0	0	1	1	10		1	0	1	1 36-2/3
0	1	0	0	13-1/3	1	1	0	0	40
0	1	0	1	16-2/3	1	1	0	1	43-1/3
0	1	1	0	20	1	1	1	0	46-2/3
0	1	1	1	23-1/3	1	1	1	1	50

*Average or peak

DECODER INPUT / DECODER INPUT

TM 11-6625-2815-14&P

c. Mark/Space Indicator Control. Comprising a NAND gate, inverter, and flip-flop, this circuit controls the lighting of the M and S LEDs (in the PERCENT DISTORTION display) which whether the percent distortion displayed represents Mark or Space distortion. The control circuit uses the DS and MSC inputs from the DISTORTION MODE switches, and TS provided form the start control and transition synchronizer.

(1) As explained in paragraph 2-5b(1), polarity of the MSC signal depends on which DISTORTION MODE switch is pressed (if BIAS/PEAK is pressed, the Mark signal is positive; if END/PEAK is pressed, the Space signal is positive). Likewise, the DS signal (derived from TB) is a logic 1 during the *second* half of each data-bit if BIAS/PEAK is pressed, and a logic 1 on the *first* half of each data-bit if END/PEAK is pressed. The TS pulse occurs on each M/S or S/M transition of the monitored data.

(2) As shown in the timing diagram (fig. 2-6), if the SIM transition occurs too early in BIAS/PEAK operation, the TS pulse is positive while DS is positive, lighting the M lamp to indicate Marking bias. Similarly, if the SIM transition occurs too late, the TS pulse is positive when the DS pulse is *negative,* lighting the S lamp to indicate Spacing bias.

(3) In END/PEAK operation, the action is essentially identical, except that M/S transitions control lighting of the M or S lamp.

d. Parity Detector. The parity detector provides a PARITY ERROR indication, on a character-basis, in either 7- or 8-level code operation; a strapping option enables detection of either odd- or even-parity errors.

(1) Four inputs are supplied to the parity detector: clear, end-of-data plus 1/2 bit, MI, and TB. The clear input resets the circuit at the beginning of each character's start-Space. With the circuit initially cleared, MI and TB inputs are then used in the actual parity error detection.

(2) MI is a logic 1 for each Space bit appearing in the monitored data. The TB input is differentiated so that it produces a pulse in the middle of each data-bit period whether or not any MIS or SIM transition has occurred (e.g., the input data may remain in a Space condition for three bit periods, but this would still produce three differentiated TB pulses). The MI and TB inputs are used to count the number of Space bit-periods in the monitored data, by alternately setting and resetting a flip-flop for each such period. If the circuit is strapped for even polarity and an even number of Space bit-periods are counted, a parity error is indicated. If strapped for odd parity and an odd number of Space bit-periods are counted, a parity error is also indicated.

(3) The parity detector output is not enabled until an end-of-data plus 1/2 bit signal is received from the character distributor. If a parity error has been detected, the parity detector outputs a logic 0, lighting the

PARITY ERROR lamp; the lamp remains lighted until the RESET pushbutton is pressed and released.

3-7. DISCRETE COMPONENT CIRCUITS-DETAILED DESCRIPTIONS

INPUT INTERFACE (fig. FO-1) circuit comprising transistors Q1 and Q2, and three inverters which are part of IC U14, converts all types of inputs to logic levels of 0 and + 5 volts and generates the MI, MSP, and BP signals used in the Data Analyzer.

a. All Data Analyzer inputs are converted to 6-volt pulses at the C11R14 junction.

(1) Low-level polar (positive Mark) signals are normally at this amplitude; therefore, they require no conversion and are applied directly to the junction through R12 and S5A.

(2) In high-level polar (nominally 20ma) or 20ma neutral operation, the 20ma input is converted to 6 volts across R24 (with applicable switch S2 or S4 pressed) and applied to the junction through R13.

(3) For 60ma neutral operation, with S3 pressed, the input is converted to 6 volts across R25, and is applied to the junction through R13.

b. C11/14 function as an integrator to filter out transients present in the input; the resulting signal is applied to the base of amplifier Q1 across diodes CR1-CR2 which, in polar operation, are referenced to 4.3 volts established by Zener diode VR2. This 4.3-volt dc level also serves as the return reference for the external + 6-volt polar input (via REV switch S5) so that *M*IS inputs actually vary between 10.3 and - 1.7 volts.

(1) However in polar operation, CR1-CR2 limit the Q1 base signal input to voltage swings between approximately 3.6 and 5 volts. With the Q1 emitter referenced to approximately 5 volts by VR2, CR3, and R17, Q1 is cut off when the base input rises above 4.3 volts (Mark). As the input drops below 4.3 volts (Space), Q1 is driven into conduction. Output form the Q1 collector is a negative Mark (ground) and a positive Space (5 volts).

(2) Neutral operation is essentially the same as polar, except that, for neutral signals, common return is referenced to ground through R2-R21 and S4A; R2-R21 provide half-current slicing to establish a 3volt Mark/Space switchover reference.

NOTE

With negative Mark low-level polar (or negative-tip high-level polar/neutral inputs), REV switch S5 is pressed and input signals are applied to the emitter of Q1, producing ground/5-volt outputs at the Q1 collector.

c. Outputs from Q1 are applied to the base of switch Q2. With a ground (Mark) input, the Q2 collector is at 10 volts; with a 5-volt (Space) input, the collector is at

3-8
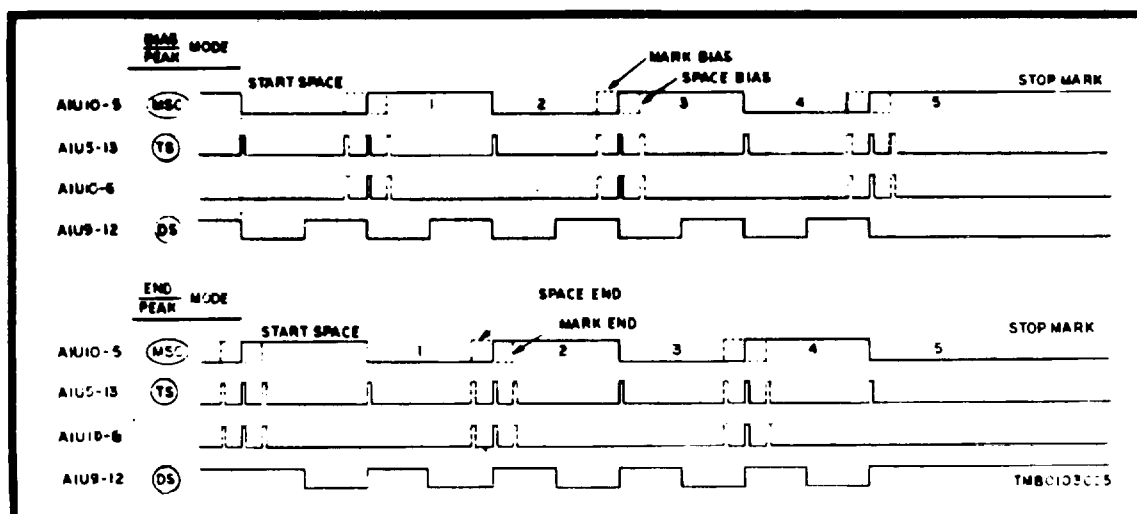
MARK/SPACE INDICATOR CONTROL, TIMING DIAGRAM

EL2PQ007

Figure 3-3. Mark/Space Indicator Control, Timing Diagram.

0 volt. The collector output is: coupled back to the Q1 base through hysteresis feedback resistor R16, to provide greater noise immunity; and applied to inverter input U14-3 and differentiator C7-R22. The inverted output (negative Mark) from U14-4 (MI) is fed to differentiator C6-R20, whereas the positive Mark signal appears at C7-R22. MI, which lights the DATA MARK lamp (indicating presence of a positive Mark input) is used in the Data Analyzer parity detector circuit as described in paragraph 3-6d.

d. Differentiator action is the same for both types of circuits, except that the circuits operate on signals of opposite polarity.

(1) Output of C6-R20 is a sharp negative pulse for each AIM transition and a sharp positive pulse for each MIS transition. The positive pulse is blocked by CR4 (part of 2-input OR gate CR4-CR5), but the negative input is coupled to inverter input U14-5.

(2) Output of C7-R22 is a positive pulse for each S/M transition and a negative pulse for each *MIS* transition. The positive pulse is blocked by CR5 so that only the negative pulse is applied to U14-5. The resultant inverted output at U14-6 is a stream of positive pulses representing M/S and SIM transitions of the input data. This BP signal is used in the Data Analyzer timing and control circuits as described in paragraph 3-4.

e. The differentiated output from C7-R22 is also applied to inverter input U14-1. Since the U14-1 input is normally held at + 5 volts, applied through R22, only the negative-going pulse has any effect, producing a positive pulse at U14-2. Representing M/S transitions of the

input data, this pulse (designated "MSP') is used in the Data Analyzer timing and control circuits as described in paragraph 3-4.

3-8. POWER SUPPLY INVERTER (fig. FO-1)
This circuit, which receives a 5-volt dc input from the battery, supplies + 10-volt dc outputs and a + 6-volt dc output for use in various circuits of the Data Analyzer. Battery input is applied to astable multi-vibrator Q2Q3, which generates a 50kHz squarewave the peak-to-peak amplitude of which is approximately 20 volts.

a. Coupled through transformer T1 to bridge rectifier CR1-CR4, the squarewave results in production of + 10- and - 10-volt dc outputs (from opposite sides of the bridge rectifier). These dc outputs are filtered by capacitors C6 and C7.

b. The + 6-volt dc output is produced by initially stepping down the 10-volt dc output to approximately 8 volts, across Zener diodes A2VR1 and VR2 (fig. FO-2), and reapplying the 8 volts to Assembly Al where it is further reduced to 6 volts across Zener diode VR2.

3-9. BATTERY TEST CIRCUIT (fig. FO-1)
The battery test circuit comprises transistor Q1, RESET switch S7, and PARITY ERROR lamp DS1.

a. When RESET switch S7 is pressed, the 5-volt battery provides collector voltage for Q1 through PARITY ERROR lamp DS1 and is connected across 4.3 volt Zener diode VR1 and resistor R25 in the Q1

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base circuit. If battery voltage exceeds 4.3 volt, VR1 conducts and the voltage drop across R25 turns ON Q1, lighting the PARITY ERROR lamp. The higher the charge condition of the battery, the more heavily Q1 conducts, increasing the intensity of PARITY ERROR lamp brightness.

b. If the battery is excessively discharged so that its voltage does not exceed the VR1 breakdown voltage, ' 1 is cut off and the PARITY ERROR lamp is not lighted.

c. Fuse F3, connected in series with a battery across the 5 volt dc input (fig. FO-1), serves as a safety device to protect the battery if an overload (short circuit) condition occurs.

SECTION IV

MAINTENANCE

4-1. MAINTENANCE PRACTICES
Except for replacement of the battery and fuses, the Data Analyzer should be returned to the factory for service. Where field service is necessary, it should be performed only by an engineer or technician thoroughly familiar with operation of the unit and experienced with similar equipment. The performance test described in table 4-2 can serve to establish the unit's general operating condition. If the unit malfunctions, signal trace using the waveforms shown in figures 3-2 and 3-3 and the diagrams provided in figures FO-1, FO-2, and 4-1. Perform the frequency adjustments as required, as described in paragraph 4-5. To select parity mode, baud-rate, 7- or 8-level code, and ac power input other than those factory strapped, proceed as described in paragraph 4-6. *a. Battery Replacement.* If the battery cannot be brought up to a fully charged condition as described in paragraph 2-6, replace the battery as follows:
(1) Remove the three screws (two near the carrying handle hinges, and one at rear of unit) that fasten top of Data Analyzer case to bottom of unit.
(2) Lift cover off unit, gently rocking cover back and forth; make sure not to force cover against DATA MARK or PARITY ERROR lamp or pushbuttons in top of unit or output jacks in front of unit.
(3) Remove battery from holder.
(4) Remove red plastic caps from each end of battery.
(5) Unsolder wire from terminal on each end of battery, and solder wires to replacement battery (black to negative, white to positive).
(6) Replace plastic caps on battery.
(7) Replace battery in holder; be careful not to pinch wires.
(8) Carefully replace top cover, front first, making sure that the DATA MARK and PARITY ERROR lamps come

through holes in cover.
(9) Replace and tighten the three security screws.
b. Fuse Replacement. To replace the ac input or high-level loop fuses (bottom of the unit, (fig 2-1), unscrew the fusecap and extract the fuse (fuse is equipped with two pins that plug into holder). Insert new 0.1-ampere fuse, and replace cap. Replace battery fuse F3 (see fig. 4-5) as follows.
(1) Remove the three screws (two near the carrying handle hinges, and one at rear of unit) that fasten top of Data Analyzer case to bottom of unit.
(2) Lift cover off unit, gently rocking cover back and forth; make sure not to force cover against DATA MARK or PARITY ERROR lamp or pushbuttons in top of unit or output jacks in front of unit.
(3) Remove four screws that fasten bottom cover of Data Analyzer and remove cover.
(4) Remove fuse, located under battery holder bracket, and insert new 1-ampere fuse.
(5) Replace and tighten bottom cover in position, using four securing screws.
(6) Carefully replace top cover; front first, make sure that the DATA MARK and PARITY ERROR lamps come through hole in cover.
(7) Replace and tighten the three securing screws.

4-2. TEST EQUIPMENT REQUIRED
The test equipment listed in table 4-1 is required for maintenance of the Data Analyzer. Manufacturer and model recommendations are typical; equivalent types may be substituted. The *Common Name* column specifies the name by which each test equipment is subsequently referred to.

Table 4-1. Test Equipment Required

Name	Common Name	Function
Electronic Frequency Counter, Hewlett-Packard Model HP, 5211A or equivalent	Counter	Measurement of time-base frequencies and bit rates.
Oscilloscope, Tektronix Model 535A, or equivalent	Oscilloscope	Waveform observation and measurement Also used for signal tracing.
Multimeter, Simpson Model 260, or equivalent	Multimeter	General voltage and resistance and measurements.
Pattern Generator, STELMA Model PG-303A, or equivalent	PG-303A	Generation of telegraph distortion test patterns.

4-3. PERFORMANCE TEST
No one combination of control settings will provide a comprehensive test of the Data Analyzer; therefore, a thorough Performance Test requires that the various functional sections of the unit be tested and evaluated

separately. The performance test outlined in table 4-2 is designed to check the unit in a logical series of separate tests; successful completion of the test verifies equipment operational capability and can serve to define trouble symptoms.

DATA ANALYZER WIRING DIAGRAM, AND DECODER AND DISPLAY CIRCUITS ASSEMBLY A3 SCHEMATIC DIAGRAM
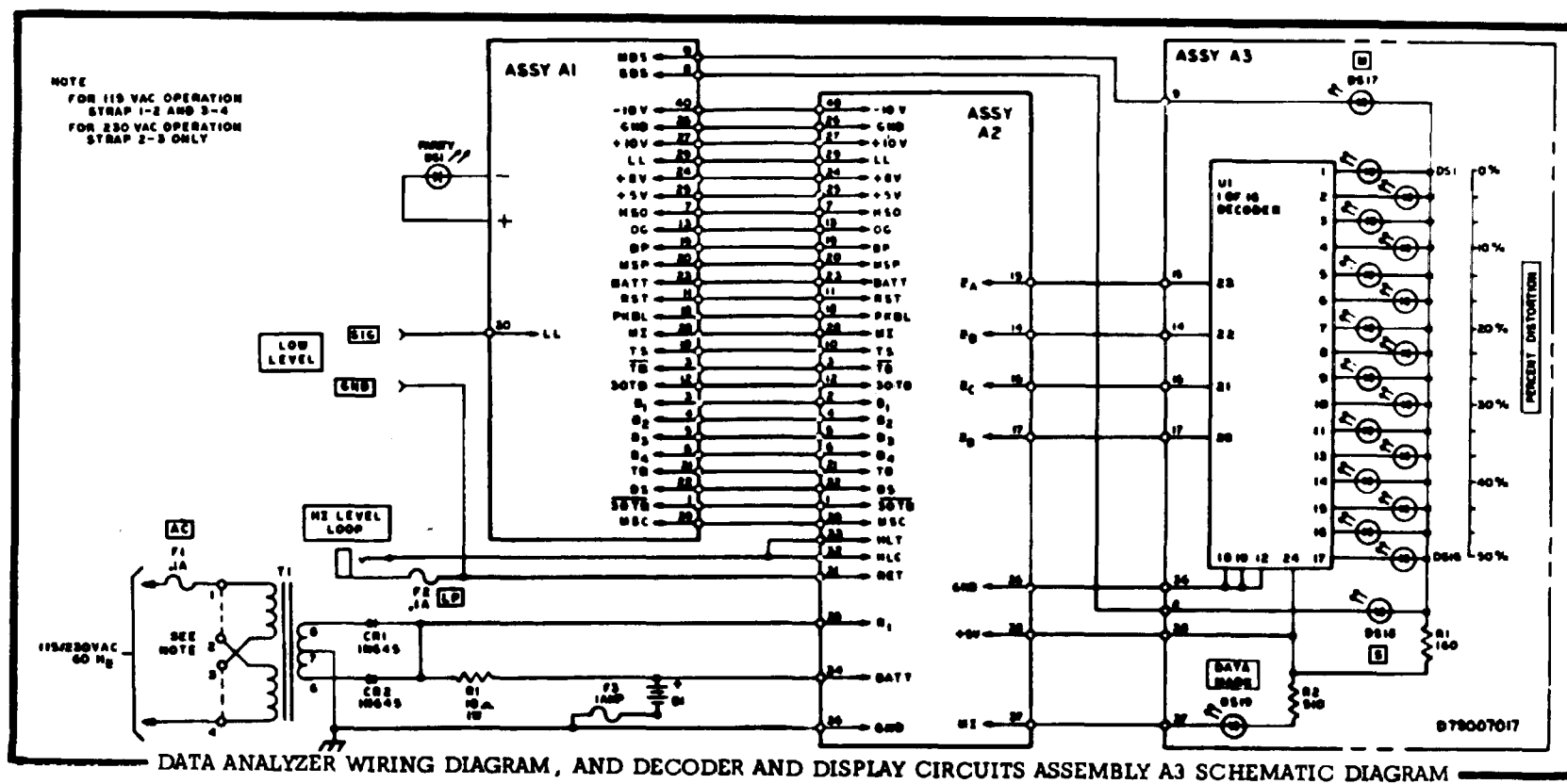
EL2PQ010

Figure 4-1. Data Analyzer Wiring Diagram, and Decoder and Display Circuit Assembly A3 Schematic Diagram.

Table 4-2. Performance Test

Procedure	Normal Indication

BATTERY TEST
    1. Press and hold RESET switch,
    2. Observe PARITY ERROR lamp.
 	
    3. Release RESET switch.
                NOTE
    Continue remainder of test with power cord plugged into ac outlet.
	PARITY ERROR lamp glows brightly. If it does not, recharge battery for several hours before continuing tests.

DISTORTION MEASUREMENT TEST
    1. Connect LOW LEVEL output jacks of PG-303A to LOW LEVEL jacks on Data Analyzer.
    2. On Data Analyzer, press following pushbuttons:
        a. POLAR.
        b. BIAS/PEAK.
        c. Uppermost RATE pushbutton.
        d. 5 LEV.
        e. PWR.
    3. Make preliminary setup on PG-303A as follows:
        a. PATTERN-FOX MSG 5.
        b. DISTORTION PERCENT-0.
        c. DISTORTION TYPE-OFF.
        d. BIT RATE-same as Data Analyzer.
        e. MODE-FREE RUN with 1.5 UNIT STOP MARK.
        f. POWER-ON.
                NOTE
    If PG-303A is strapped for negative Mark output, press REV pushbutton on Data Analyzer.
    4. On Data Analyzer, press and release RESET pushbutton. Observe PERCENT DISTORTION display and DATA MARK indicator.
    5. On PG-303A, set DISTORTION TYPE switch to BIAS-M (Marking). Slowly increase DISTORTION PERCENT setting, 1 percent at a time, and observe Data Analyzer PERCENT DISTORTION display.
 	
    6. On PG-303A, set DISTORTION PERCENT to 20. On Data Analyzer, press and release RESET pushbutton and observe PERCENT DISTORTION display.
    7. On PG-303A, momentarily set DISTORTION PERCENT to 30 and then back to 20. Observe Data Analyzer PERCENT DISTORTION display.
    8. On Data Analyzer, press and release RESET pushbutton and observe PERCENT DISTORTION display.
    9. Repeat steps 1 through 8 for each of three remaining RATE switches on Data Analyzer. For each rate, change BIT RATE on PG-303A appropriately.
   10. Repeat steps 1 through 5; however, in step 5, set PG-303A DISTORTION RATE switch to BIAS-S (Spacing). Make only several distortion measurements in step 5, for a random sampling.
   11. Repeat steps 1 through 5; however, in step 2b, press END/PEAK pushbutton and, in step 5, set PG-303A DISTORTION TYPE switch to END-M (Marking). Make only several distortion measurements in step 5, for a random sampling.
   12. Repeat steps 1 through 5; however, in step 2b, press END/PEAK pushbutton and, in step 5, set PG-303A DISTORTION TYPE switch to END-S (Spacing). Make only several distortion measurements in step 5, for a random sampling.
   13. Remove connections from LOW LEVEL jacks on Data Analyzer and PG-303A.
   14. With PG-303A connected for high-level polar operation, set HI-LEVEL SELECT switch to POLAR, and connect HI-LEVEL jack on PG-303A to HI LEVEL LOOP jack on Data Analyzer.
   15. Repeat steps 2 through 5; however, in step 5, make only several distortion measurements, for a random sampling.
	0 percent distortion, with DATA MARK indicator flickering.
	
	M indicator ON. PERCENT DISTORTION indication same as PG-303A setting, to nearest 1-2/3
	            NOTE
	    Depending upon combined accuracies of PG-303A and Data Analyzer, the PERCENT DISTORTION indication may indicate either next lowest or highest value.
	20 percent distortion.
	
	20 percent distortion, average.
	30 percent distortion.
	20 percent distortion.
	
	Same as above.
	
	Same as above, except indicator should be ON.
	
	Same as above.
	
	Same as above, except S indicator should be ON.
	
	Same as above.

Table 4-2. Performance Test-Continued

Procedure	Normal Indication
16. With PG-303A connected for 20 or 60ma neutral operation, set HI LEVEL SELECT swtich to NEUT, and connect HI-LEVEL jack on PG-303A to HI-LEVEL LOOP jack on Data Analyzer.	
17. Repeat steps 2 through 5; however, in step 2a, press 20 MA or 60 MA pushbutton as applicable and, in step 5, make only several distortion measurements, for a random sampling.	Same as above.
NOTE	
If Data Analyzer is equipped for 8-level operation, proceed to step 18. If Data Analyzer is equipped for 7-level operation, proceed to step 19.	
18 Repeat steps 2 through 5; however, in step 2d, press 8 LEV pushbutton and, in step 3a, set PATTERN switch to FOX MSG 8 Make only several distortion measurements in step 5, for random sampling.	Same as above.
19. Repeat steps 2 through 5; however, in step 2d, press 7 LEV pushbutton and, in step 3a; make the following settings: a. PATTERN-SELETED CHARACTERS CODE LEVEL 7. b. SELECTED CHARACTERS-press pushbuttons 1,3, 5, and 7 in vertical column 1. c. CHARACTER SEQUENCE LENGTH--press pushbutton I Make only several distortion measurements in step 5 for random sampling 20. Remove connections between HI LEVEL LOOP jack on Data Analyzer and HI-LEVEL jack on PG-303A.	Same as above.
PARITY-ERROR CHECK 1. Connect LOW LEVEL output jacks of PC-303A to LOW LEVEL jacks on Data Analyzer. 2. On Data Analyzer, press following pushbuttons: a. POLAR. b. BIAS/PEAK. c. Uppermost RATE pushbutton. d. 7 LEV or 8 LEV, as applicable. e. PWR 3. Make preliminary setup on PG-303A as follows- a. PATTERN-SELECTED CHARACTERS CODE LEVEL 7 or 8, as applicable. b SELECTED CHARACTERS-if Data Analyzer is strapped for even parity, press pushbuttons 1, 3, 5, and 7 in vertical column 1; if strapped for odd parity, press pushbuttons 1, 3, and 5. c. CHARACTER SEQUENCE LENGTH-press pushbutton 1 d. DISTORTION TYPE-OFF. e. DISTORTION PERCENT-0. f. BIT RATE-Same setting as that of Data Analyzer g. MODE-FREE RUN, with 1.5 UNIT STOP MARK h. POWER-ON. **NOTE** If PG-303A is strapped for negative Mark output, press REV pushbutton on Data Analyzer.	
4. On Data Analyzer, press and release RESET pushbutton. Observe PARITY ERROR and DATA MARK indicators.	PARITY ERROR indicator OFF, with DATA MARK indicator flickering.
5. On PG-303A, release pushbutton 1 of SELECTED CHARACTERS. Observe PARITY ERROR indicator on Data Analyzer.	PARITY ERROR lamp ON.
6. ON PG-303A, press pushbutton 1 of SELECTED CHARACTERS.	
7. On Data Analyzer, press RESET pushbutton and observe PARITY ERROR indicator.	PARITY ERROR indicator OFF.
8. Remove connections between PG-303A LOW LEVEL, and Data Analyzer LOW LEVEL jacks.	

4-4. REPAIR

a. Repair and replacement of Data Analyzer components may be accomplished using standard techniques and practices, including precautionary measures required when replacing semiconductors and integrated circuits.

b. Parts location diagrams for components mounted on PC cards AI, A2, and A3 are shown in figures 4-2, 4-3, and 4-5; locations of components not mounted on the PC cards and not otherwise identified by frontpanel nomenclature are shown in figure 4-5. In most cases, component replacement will not necessitate re

calibration or readjustment of the unit, if an exact replacement part has been used. However, if any parts in the time base oscillator on PC card Al are replaced, perform the adjustment procedure provided in paragraph 4-5 to check for proper output frequencies.

4-5. TIME BASE OSCILLATOR FREQUENCYADJUSTMENT
The time base oscillator output frequency should be

checked or adjusted whenever an oscillator circuit component is replaced or incorrect bit timing is suspected. Take all frequency measurements with a counter connected to TP1 on PC card Al (fig. FO-1); the appropriate frequency for each baud-rate is listed below (if the frequency for a selected baud rate is not as specified, adjust the appropriate control to obtain the proper frequency-see figure 4-2 for locations of adjustment controls A1R1-A1R4.

Baud Rate*	Frequency (Hz) Measured at A1PT1)
37.5	9000
40	9600
45	10,920
50	12,000
56.8	13,639
61	14,673
66	16,000
70	16,800
74	17,808
75	18,000

Baud Rate	Frequency (Hz) (Measured at A1PT1)
82.5	9900
96	11,520
100	12,000
105	12,600
110	13,200
134.5	16,140
148.5	17,820
150	18,000
192	11,520
200	12,000
300	18,000

*Refer to RATE switch location, below, to identify corresponding adjustment control.

RATE Switch Location	Adjustment Control
Upper	A1R1
Upper-Middle	A1R2
Lower-Middle	A1R3
Lower	A1R4

4-6. STRAPPING OPTIONS
Although the Data Analyzer is shipped from the factory with all customer specified strapping options included, these options may be changed in the field to satisfy requirements of different applications and uses. PC card A1 has strapping options to select odd-or even-parity error checks, 7- or 8-level code operation, and baud-rate. A strapping option on power transformer T1 allows operation from a 115- or 230volt ac source. Strapping connections required to obtain the desired characteristics for these options are described below. Refer to figures 4-2 and 4-4 for location of strapping terminals on PC card Al and the location of transformer T1, respectively.

a. Parity Mode. A choice of odd- or even-parity error detection in 7- or 8-level coded inputs is available.

(1) For 8-level even parity or 7-level odd parity, strap E to F.

(2) For 8-level odd parity or 7-level even parity, strap D to F.

b. 7- or 8-Level Code Operation. The Data Analyzer can monitor either 7- or 8-level code inputs, besides the 5-level code.

NOTE
When changing from one code level to another, the appropriately labeled pushbutton (with the 7 LEV or 8 LEV designation) should be ordered from Data Products Telecommunications Division for installation on switch S6; the applicable Part No. for each pushbutton is

identified below, with the strapping directions.

(1) For 8-level code operation, strap G to H (8 LEV pushbutton, Part No. 45005108-007).

(2) For 7-level code operation, strap J to H (7 LEV pushbutton, Part No. 45004108-035).

c. Baud-Rate. Strapping capability is provided to change the particular baud-rate selected by any one of the four RATE switches. Baud-rate strapping is effected by connecting any one of three terminals (A, B, or C) to any one of terminals 1, 2, 3, and 4. While more than one connection may be made to any of terminals A, B, or C (depending upon the baud-rates selected), only one connection may be made to each of terminals 1, 2, 3, and 4 (since these terminals correspond to RATE switches S1, S2, S3, and S4, respectively-and, obviously, one switch can select only one baud-rate). Besides changing strapping connections, a baud-rate conversion kit must be used (available from Data Products, Telecommunication Division) to effect baud-rate changes. This kit contains resistors of proper value for R6 through R9, and a pushbutton labeled with the corresponding baud-rate. Strapping connections for selecting baud-rate ranges and conversion kit part numbers are charted below. After the conversion kit has been installed and the strapping has been accomplished, make fine frequency adjustments as described in paragraph 4-5.
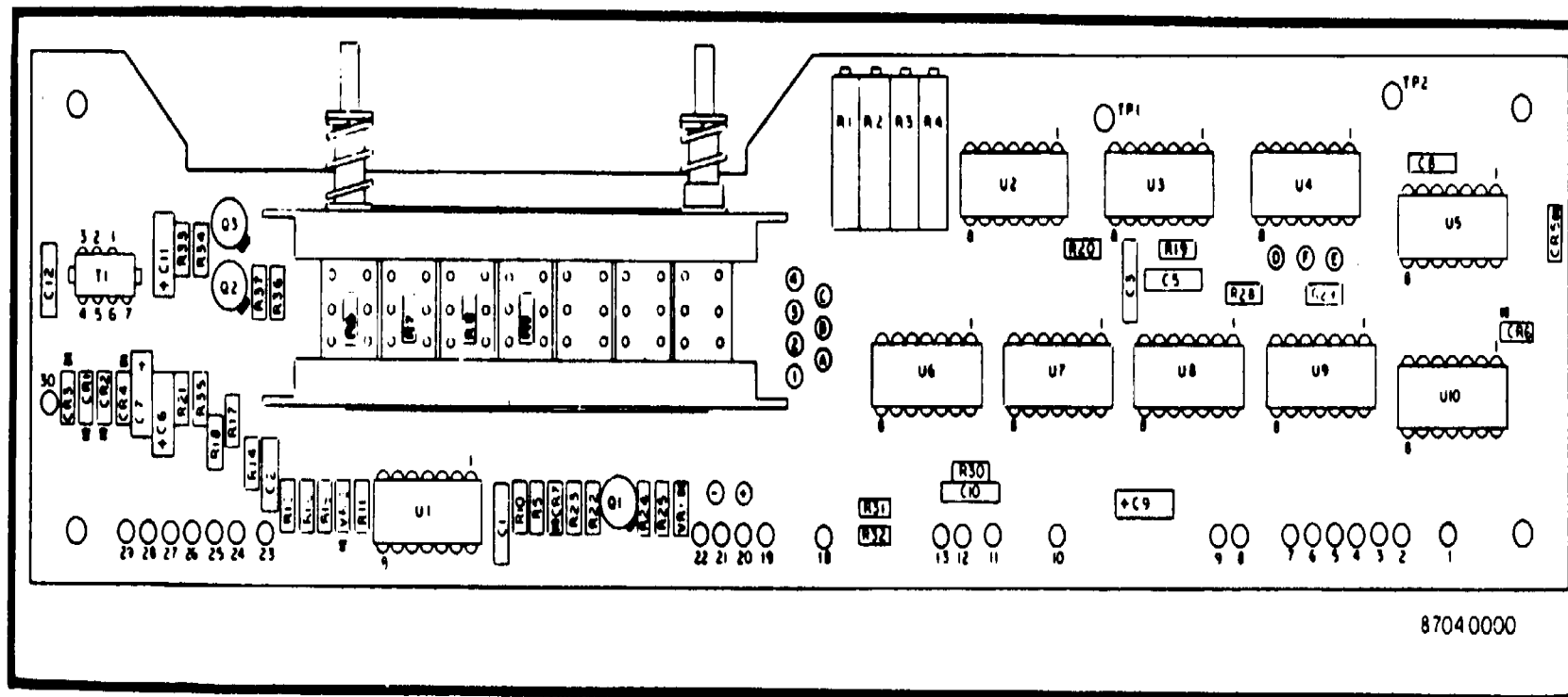
TIMING, PARITY, AND POWER ASSEMBLY A1, COMPONENT LOCATION DIAGRAM

EL2PQ011

Figure 4-2. Timing, Parity, and Power Assembly A1, Component Location Diagram.
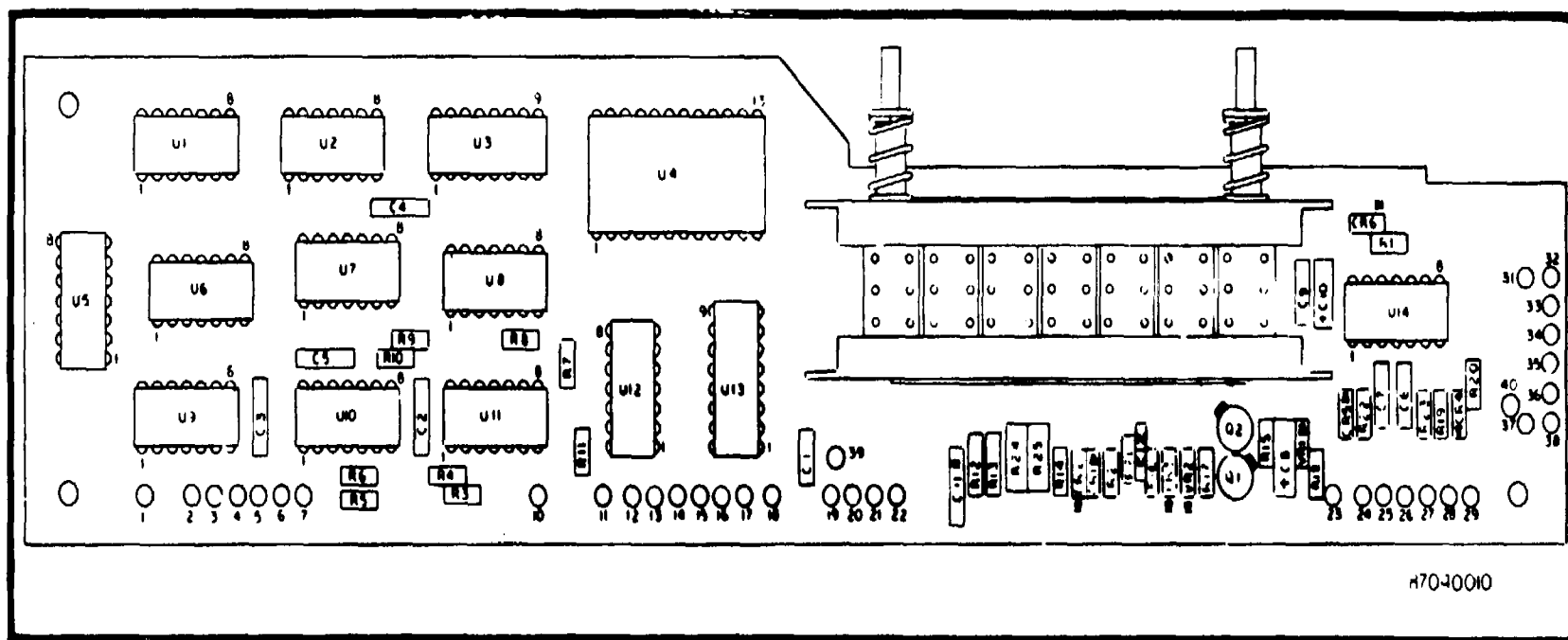
DISTORTION MEASURING CIRCUIT ASSEMBLY A2, COMPONENT LOCATION DIAGRAM

EL2PQ012

Figure 4-3. Distortion Measuring Circuit Assembly A2, Component Location Diagram.

Baud-Rate	Strap to Terminal 1,2,3,or4
37.5	C
40	C
45	C
50	C
56.8	C
61	C
66	C
70	C
74	C
75	C

Baud-Rate	Strap to Terminal 1,2,3,or4
82.5	B
96	B
100	B
105	B
110	B
134.5	B
148.5	B
150	B
192	A
200	A
300	A

Baud-Rate	Conversion Kit Part No. 24007006
37.5	-000
45	-001
74	-002
110	-003
150	-004
40	-005
50	-006
56.8	-007
61	-008
66	-009

Baud-Rate	Conversion Kit Part No. 24007006
70	-010
75	-011
82.5	-012
96	-013
100	-014
105	-015
134.5	-016
148.5	-017
192	-018
200	-019
300	-020

d. *AC Power Input.* The Data Analyzer can operate with either a 115- or 230-volt ac input, depending on power transformer T1 strapping (fig. 4-7). To operate from:

(1) 115 volts, strap T1 terminal 1 to 2, and 3 to 4.
(2) 230 volts, strap only T1 terminals 2 to 3.

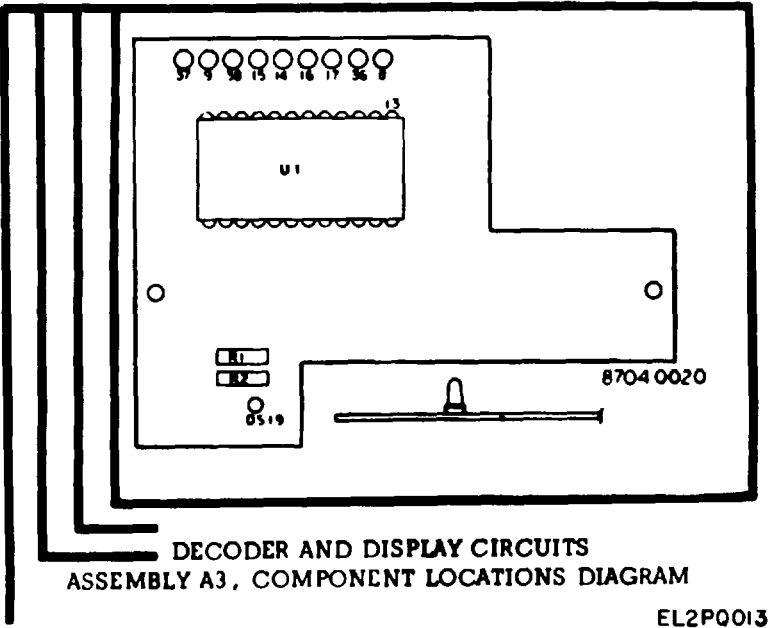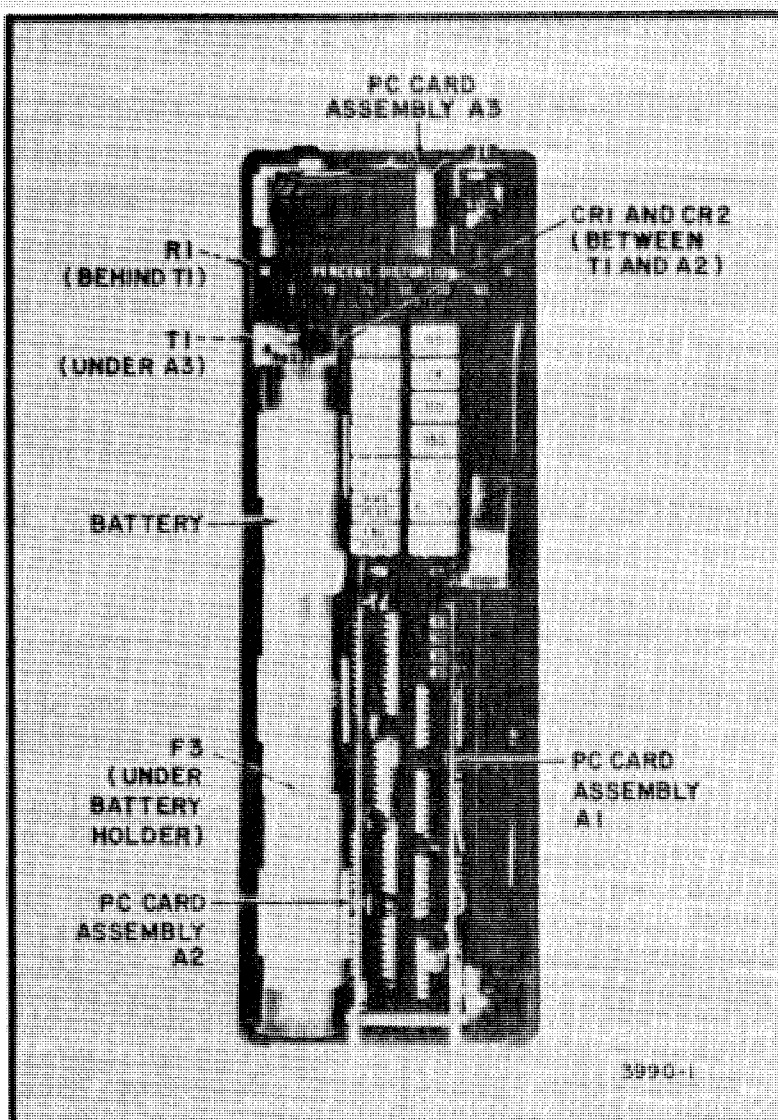DECODER AND DISPLAY CIRCUITS ASSEMBLY A3, COMPONENT LOCATIONS DIAGRAM

EL2P0013

Figure 4-4. Decoder and Display Circuits Assembly A3, Component Locations Diagram.

Figure 4-5. Data Analyzer Top View, Component Locations.

4-9

SECTION V

PARTS LIST

5-1. GENERAL

A complete list of replaceable Data Analyzer electronic parts by major assembly is provided in table 5-2. Parts are listed in alphanumeric order, by reference designation symbol, within each assembly breakdown. A brief description and the manufacturer part and code numbers are provided for each entry. Manufacturer codes are identified in table 5-1.

Table 5-1. Manufacturer Codes

Code No.	Manufacturer
01295	Texas Instruments Inc., Semiconductor and Components Division, Dallas, Texas
07263	Fairchild Camera and Instrument Corp, Semiconductor Division, Mountain View, California
29083	Monsanto Co. Inc., Santa Clara, California
32997	Bourns Inc., Trimpot Products Division, Riverside, California
34122	Marathon Battery Co., Cold Spring, New York
56289	Sprague Electric Co., North Adams, Massachusetts
70903	Belden Corp., Chicago, Illinois
71400	Bussmann Mfg Division of McGraw Edison Co., St. Louis, Missouri
75915	Littelfuse Inc., Des Plaines, Illinois
81349	Military Specifications
82389	Switchcraft Inc., Chicago, Illinois
83330	Herman H. Smith Inc., Brooklyn, New York
84171	Arco Electronics Inc., Great Neck, New York
86684	RCA Corp., Electronics Components Harrison, New Jersey
86238	STELMA, Inc., Stamford, Connecticut

Table 5-2. Replaceable Parts

PORTABLE ANALYZER (97040000-0000)

Ref. Desig.	Description	Mfr's Part No.	Mfr's Code No.
A1	CHASS ASSY	97040001-000	96238
BT1	BTRY, NL-CAD: 4.8V	38929-10	34122
CR1,CR2	SEMICOND,DIO:	1N645	81349
PI,P2	FUSE,CRTG: 1110 Amp;	GMW1-10	71400
P3	FUSE,CRTG:1 Amp;	212001	79515
P3	FUSE,CRTG:1 AMP	312001	75915
R1	RES,FXD,COMP: 10 ohms,± 5%,1W;	RC32GF100J	81349
T1	XFMRPWR:	43000290-000	96238
W1	CABLE ASSY,PWR,ELEC:	17106S	70903
XF1,XF2	FUSE HLDR	HWA-AF	71400
XF3	FUSE HLDR	3823-1	71400

CHASSIS ASSEMBLY A1 (97040001-000)

Ref. Desig.	Description	Mfr's Part No.	Code No.
AI	CKT CARD ASSY: Timing, parity and power;	87040000-000	96238
A2	CKT CARD ASSY: Distortion measuring;	87040010-000	96238
A3	METER ASSY	97040002-000	96238
DS1	SEMICOND,DIO: Light emitting;	MV5022	29083
J1	JACK,TEL:	NL111	82389
TP1	JACK,BANANA: Red;	1508-102	83330
TP2	JACK,BANANA: Black;	1508-103	83330

Table 5-2. Replaceable Parts-Continued

CIRCUIT CARD ASSEMBLY A1A1, TIMING, PARITY & POWER (87040000-000)

Ref. Desig.	Description	Mfr's Description	Mfr's Part No.	Code No.
CR1-CR4	SEMICOND,DIO: Germanium;	1N277	81349	
CR5-CR7	SEMICOND,DIO: Silicon;	1N4148	81349	
C1	CAP.,FXD,MICA: 1000pf, ± 5%,500V;	CM06FD102J03	81349	
C2	CAP.,FXD,MICA: 220pf,± 10%,500V;	DM15E221K0O 500WV4CR	84171	
C3	CAP.,FXD,MICA: 390pf,± 10%,500V;	DM15E391KO 500WV4CR	84171	
C4	Not used			
C5	Same as C3			
C6,C7	CAP.,FXD,ELCTLT: 1uf, ± 20%,35V;	CS13BF105M	81349	
C8	CAP.,FXD,MICA: 680pf, ± 10%,300V;	DM15E681KO 300WV4CR	84171	
C9	Same as C6			
C10	CAP ,FXD,CER: O.Oluf, ± 20%,100V;	C023B101F10 3M	56289	
C11	CAP.,FXD,ELCTLT: 3.3uf,± 20%,15V;	CS13BD335M	81349	
C12	Same as C10			
DS1	SEMICOND DIO: Light emitting:	MV5022	29083	
Q1-Q3	XSTR: NPN;	2N2222	81349	
R1-R4	RES,VAR: 10K ohms, 3/4W;	3006P1-103	32997	
R5	RES,FXD,PFLM: 11.3Kohms,± 1%,1/10W;	RN55E1132F	81349	
R6-R9	RES,FXD,FILM: (Factory Selected per baud rate);	RN55CXXXXF	81349	
R10	RES,FXD,FILM: 301K ohms,± 1%,1110W;	RN55C3013F	81349	
R 11	RES,FXD,COMP: 22K ohms,+ 5%,1/4W;	RC07GF223J	81349	
R12	RES,FXD,COMP: 510 ohms,+ 5%,114W;	RC07GF511J	81349	
R13	Not used			
R14	RES,FXD,COMP: 300K ohms,± 5%,114W;	RC07GF304J	81349	
R15	RES,FXD,COMP: 10K ohms,± 5%,1/4W;	RC07GF103J	81349	
R16	Same as R11			
R17	RES,FXD,COMP: 1K ohms,: 5%,1/4W;	RC07GF102OW	81349	
R18	Same as R11			
R19	RES,FXD,COMP: 4.7K ohms,+ 5%,114W;	RC07GF472J	81349	
R20	RES,FXD,COMP: 6.8 ohms,± 5%,114W;	RC07GF682J	81349	
R21	RES,FXD,COMP: 36K ohms,± 5%,114W;	RC07GF363J	81349	
R22	Same as R12			
R23	RES,FXD,COMP: 100 ohms,± 5%,1/4W;	RC07GF101J	81349	
R24	RES,FXD,COMP: 270 ohms,± 5%,1/4W;	RC07GF271J	81349	
R25	Same as R23			
R26,R27	Not used			
R28	Same as R19			
R29	Same as R20			
R30	Same as R19			
R31	RES,FXD,COMP: 22 ohms,+ 5%,1/4W;	RC07GF220J	81349	
R32	Same as R20			
R33,R34	RES,FXD,COMP: 27K ohms,± 5%,114W;	RC07GF273J	81349	
R35-R37	RES,FXD,COMP: 15K ohms,± 5%,1/4W;	RC07GF153J	81349	
S1	SW ASSY: Rate;	46027673-000	96238	
T1	XFMR,PLS: 4.8V;		43003048-000	96238
U1	IC: COS-MOS gate;	CD4001AE	86684	
U2	IC: 4 Bit binary counter;	SN74L93N	01295	
U3	IC: Hex inverter;	SN74L04N	01295	
U4,U5	IC: DUAL J-K flip-flop;	SN74L73N	01295	
U6	Same as U2			
U7	IC: 4 Input NAND gate;	SN74L20N	01295	
U8	Same as U2			
U9	IC: Trig flip-flop;	SN74L74N	01295	
U10	IC: 2 Input NAND gate;	SN74LOON	01295	
VR1	SEMICOND DIO: Zener	1N749A	81349	
VR2	SEMICOND DIO: Zener	1N753A	81349	
CR1 -CR5	SEMICOND DIO: Silicon;	1N4148	81349	
CR6	SEMICOND DIO: Germanium;	1N277	8134'	

Table 5-2. Replaceable Parts - Cont.

Ref. Desig.	Description	Mfr's Part No.	Mfr's Code No.
C1	CAP.,FXD,MICA: 430pf, ± 10%,500V;	DM15E431K	84171
C2	CAP.,FXD,MICA: 390pf, ± 10%,500V;	DM15E91K	
		0500W4CR	84171
C3	CAP.,FXD,CER: 0.002uf , ± 20%,	C023B102F20	56289
	1000V;	2M	
C4-C7	Same as C2		
C8	CAP.,FXD,ELCTLT:3.3uf,± 20%,1V;	CS13BD335M	81849
C9	CAP.,FXD,CER; 0.01uf, ± 20%.OOV;	C023B101F10	56289
C10	Same as C8		
C11	Same as C9		
C12	CAP.FXD,MICA: 51pf, ±10%, 500V;	DM15E501K	84171
Q1	XSTR: PNP;	2N2907	81349
Q2	XSTR: NPN;	2N706	81849
R1	RES,FXD,COMP: 9.1K ohms, ± 5%,1/4W;	RC07GF912J	81349
R2	RES,FXD,COMP: 36K ohms,: ± 5%,1/4W;	RC07GF363J	81849
R3	RES,FXD,COMP: 33K ohms, ± 5%, 1/4W;	RC07GF333W	81849
R4	RES.FXD,COMP: 47K ohms, ± 5%,1/4W;	RC07GF473J	81349
R3	Same as R3		
R6	Same as R4		
R7	Same as R3		
R8	Same as R4		
R9	Same as R3		
R10	Same as R4		
R11	Same as R3		
R12,R13	RES,FXD,COMP: 20K ohms,: ± 5%,1/2W;	RC20GF203J	81849
R14	RES,FXD,COMP: 5.1K ohms, ± 5%,1/4W;	RC07GF512J	81349
R1	RES,FXD,COMP: 4.7K ohms, ± 5%,1/4W;	RC07GF472J	81849
R16	RES,FXD,COMP: 470K ohms,: ± 5%,1/4W;	RC07GF474J	81349
R17	Same as R14		
R18	RES,FXD,COMP: 15K ohms, ± 5%,1/4W;	RC07GF153J	81849
R19	Same as R3		
R20	Same as R4		
R21	RES,FXD,COMP: 120 ohms: ±5%,1/4W(factory select)	RC07GF121J	81349
R21	RES,FXD,COMP: 150 ohms: ±5% ,1/4W(factory select)	RC07GF151J	81349
R21	RES,FXD,COMP: 180 ohms,: ±5%,1/4W(factory select)	RC07GF181J	81349
R21	RES,FXD,COMP: 220 ohms,: ±5%,1/4W(factory select)	RC07GF220J	81349
R21	RES,FXD,COMP: 270 ohms,: ±5%,1/4W(factory select)	RC07GF270J	81849
R21	RES,FXD,COMP: S30 ohms,: ±5%,1/4W(factory select)	RC07GF330J	81349
R21	RES,FXD,COMP: 390 ohms,: ±5%,1/4W(factory select)	RC07GF390J	81349
R22	Same as R3		
R23	RES,FXD,COMP: 120 ohms, ±5%,1/4W;	RC07GF121J	81849
R24	RES,FXD,WW: 300 ohms, ±5%,8W;	RW69V301	81849
R25	RES,FXD,WW: 100 ohms,: ±5%,3W;	RW69V101	81849
S1	SW ASSY: Rate;	46027674-000	89238
U1,U2	IC: Duel J-K flip-flop;	SN74L73N	01295
U3	IC; 4 Bit comparator	SN74L85N	01295
U4	IC: Dual 4 bit latch;	U6N93L859X	07285
US	IC: 2 input NAND gate;	SN74L00N	01295
U6-U8	IC: 4 Bit binary counter,	SN74L98N	01295
U9	IC: 2 IN exclusive OR gate;	SN74L86N	01295
U10	Same as U5		
U11	Same as U1		
U12	IC: Trig, flip-flop;	SN74L74N	0129b
U13	IC: 2 Input multiplexer;	U7B9L2259X	07283
U14	IC: Hex inverter;	SN74L04N	01295
VR1,VR2	SEMICOND DIO: Zener;	1N749A	81349

Table 5-2. Replaceable Parts-Continued

METER ASSEMBLY A1A3 (97040002-000)

Ref. Desig.	Description	Mfr's Part No.	Mfr's Code No.
A1	CKT CARD ASSY: Decoder;	87040020-000	96238
A1DS19	SEMICOND,DIO: Light emitter;	MV5022	29083
A1R1	RES,FXD,COMP: 160 ohms,± 5%,1/4W;	RC07GF161J	81349
A1R2	RES,FXD,COMP: 510 ohms, ± 5%,114W;	RC07GF511J	81349
A1U1	IC: Decoder;	U6N93L1159X	07263
A2	ELEC CMPNT BD ASSY: Meter display;	97040003-000	96238
A2DS1-A2DS18	SEMICOND,DIO: Light emitting;	MV10A	29083
A2TB1	TB:	64047015-000	96238

APPENDIX A

REFERENCES

DA Pam 310-4   Index of Technical Publications: Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA Pam 310-7   US Army Index of Modification Work Orders.
SB 38-100   Preservation, Packaging, Packing and Marking Materials, Supplies, and Equipment Used by the Army.
TB 43-0118   Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters.
TM 38-750   The Army Maintenance Management System (TAMMS).
TM 740-90-1   Administrative Storage of Equipment.
TM 750-244-2   Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

A-1

APPENDIX D

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

D-1. General.
This appendix provides a summary of the maintenance operations for Data Analyzer DA-404 (Stelma Model DA-404) It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

D-2. Maintenance Function.
Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure' in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort *(service/act*ion) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

D4. Column Entries.

a. *Column 1, Group Number.* Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. *Column 2, Component/Assembly.* Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. *Column 3, Maintenance Functions.* Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSITL coincide.

d. *Column 4, Maintenance Category.* Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate

"work time" figures will be shown for each category. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

    C-Operator/Crew
    O-Organizational
    F-Direct Support
    H-General Support
    D-Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Not applicable.

D-4. Tool and Test Equipment Requirements (Sect. III).

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

(Next printed page is D-3)

SECTION II MAINTENANCE ALLOCATION CHART
FOR

DATA ANALYZER DA-404

(1) GROUP NUMBER	(2) COMPONENT/ ASSEMBLY	(3) MAINTENANCE FUNCT.	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT.	(5) REMARKS
			C	O	F	H	D		
00	DATA ANALYZER DA-404	Inspect Test Service Install Replace Repair Overhaul	0.3 0.5 0.5			0.7 0.8 1.5	 2.0	6 1 thru 5 1 thru 5 6 6 1 thru 5 1 thru 5	
01	CHASSIS ASSEMBLY A1	Test Service Repair Overhaul				0.3 0.4 0.7	 1.0	1 thru 5 1 thru 5 1 thru 5 1 thru 5	
02	CIRCUIT CARD ASSEMBLY A1A1	Test Service Replace Repair Overhaul				0.3 0.4 0.3 0.7	 1.0	1 thru 5 1 thru 5 1 thru 5 1 thru 5 1 thru 5	
03	CIRCUIT CARD ASSEMBLY A1A2	Test Service Replace Repair Overhaul				0.3 0.4 0.3 0.7	 1.0	1 thru 5 1 thru 5 1 thru 5 1 thru 5 1 thru 5	
04	METER ASSEMBLY A1A3	Test Service Replace Repair Overhaul				0.3 0.4 0.3 0.5	 0.7	1 thru 5 1 thru 5 1 thru 5 I thru 5 1 thru 5	

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR

DATA ANALYZER DA-404

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	H,D	COUNTER, ELECTRONIC, DIGITAL READOUT AN/USM-207A	6625-00-044-3228	
2	H,D	OSCILLOSCOPE AN/USM-281C	6625-00-106-9622	
3	H,D	MULTIMETER AN/USM-223	6625-00-999-7465	
4	H,D	PATTERN GENERATOR SG-1054/G (STELMA MODEL PG 303A)		6625-00-137-7738
5	H,D	TOOL KIT, ELECTRONIC EQUIPMENT TK-100/G	5180-00-605-0079	
6	C	TOOLS AND TEST EQUIPMENT AVAILABLE TO THE OPERATOR BECAUSE OF HIS/HER ASSIGNED MISSION.		

D-4
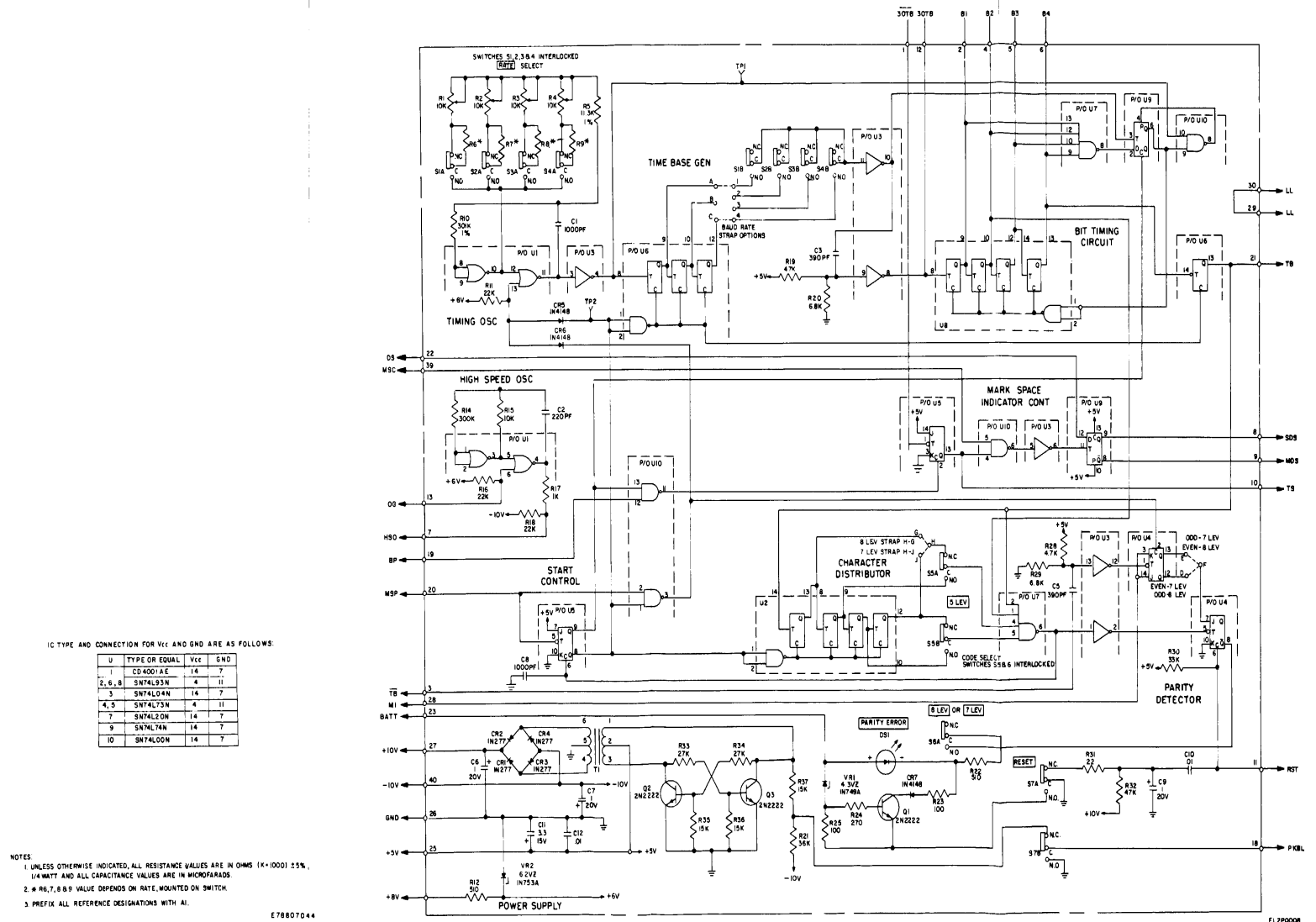
Figures FO-1. Timing, Parity and Power Assembly A1, Schematic Diagram.
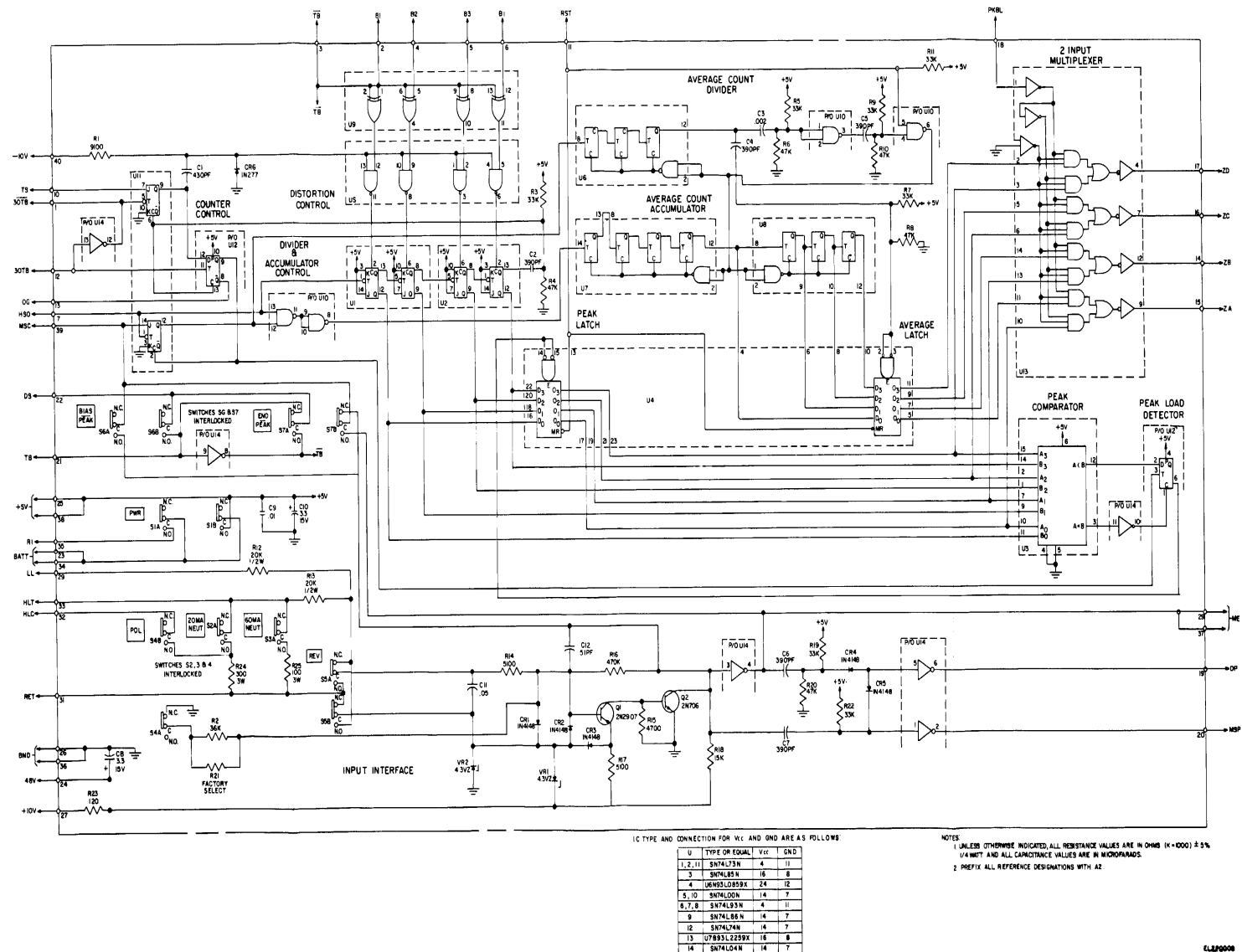
Figure FO-2. Distortion Measuring Circuits Assembly A2, Schematic Diagram.

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

THEN. . JOT DOWN THE
DOPE ABOUT IT ON THIS
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FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5825-270-10	23 Jul 81	Radio Frequency R-2176/FRN

BE EXACT. . .PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARA- GRAPH	FIGURE NO	TABLE NO.	

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER

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DA FORM 2028-2
1 JUL 79

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• ARE OBSOLETE.

P.S.—IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR
RECOMMENDATION MAKE A CARBON COPY OF THIS
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By Order of the Secretary of the Army:

E. C. MEYER
General, United States Army
Chief of Staff

Official:
J. C. PENNINGTON
Major General. United States Army
The Adjutant General

This fine document...

Was brought to you by me: