TECHNICAL MANUAL

OPERATORS, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE (INCLUDING REPAIR PARTS AND SPECIAL TOOLS LIST)

FOR

PATTERN GENERATOR PG-404 (STELMA MODEL PG-404)

HEADQUARTERS, DEPARTMENT OF THE ARMY

17 APRIL 1981

WARNING

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or on flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

CAUTION

Do not make more than one input connection at a time. Use only the appropriate input jack, and leave the other input jack unconnected.

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HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, DC, *17 April 1981*

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE (INCLUDING REPAIR PARTS AND SPECIAL TOOLS LIST) FOR PATTERN GENERATOR PG-404 (STELMA MODEL PJ-404)

Current as of 24 September 1980

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve th*is* manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN.: DRSEME-MQ, Fort Monmouth, NJ 07703.

In either case, a reply will be furnished direct to you.

Table of Contents

This manual is an authentication of the manufacturer's commercial literature which, through usage has been found to cover the data required to operate and maintain this equipment. Since the manual has not been prepared in accordance with military specifications and AR 310-3, the format has not been structured to consider levels of maintenance.

LIST OF ILLUSTRATIONS

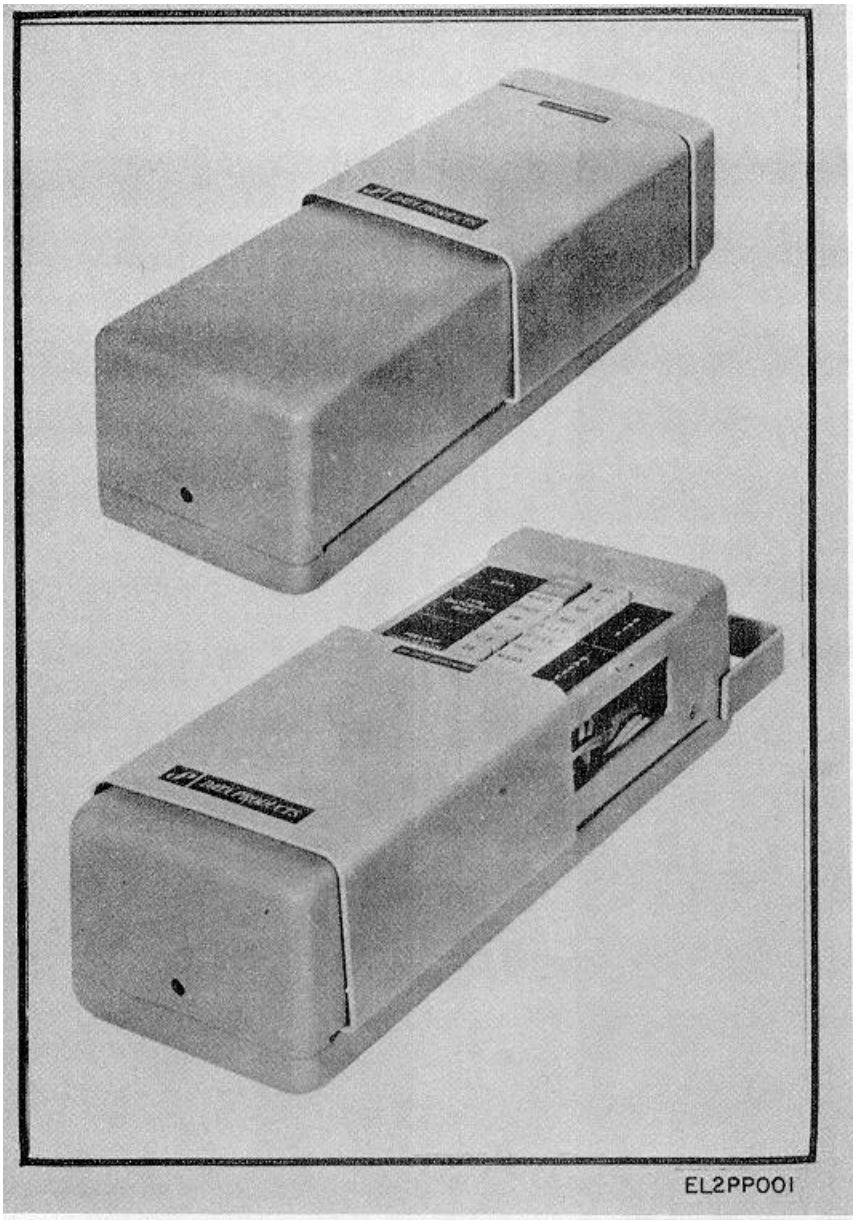

Figure 1-1. Pattern Generator Model PG-404.

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope

This manual describes Pattern Generator (Stelma Model PG-404) as a compact, portable, alternating current battery-operated test set that generates various test signal. This manual provides instructions for operation, maintenance, and performance testing. Throughout this manual, the PG-404 is referred to as Pattern Generator.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest edition of DA Pan 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7 Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

1-3. Maintenance Forms, Records, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System.

b. Report of Item and Packaging Discrepancies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73/AFR 400-54/MCO 4430.3E.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33BAFR 75-18/MCO P4610.19C and DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

If your Pattern Generator needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Tell us why a procedure is hard to perform. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703. Well send you a reply.

1-5. Administrative Storage

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed before storing. When removing the equipment from administrative storage , the performance test and adjustment procedure should be performed to assure operational readiness. Original packing case may be used when repacking equipment for shipment for repair.

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Section II. DESCRIPTION AND DATA

1-7. Purpose and Use

The Pattern Generator PG-404 is a compact, portable, ac/battery-operated test set that generates various telegraph test signal patterns hang predetermined and controllable characteristics. The Pattern Generator is designed for use with associated data measuring instruments (such as Data Products' Data Analyzer DA-404) to test and evaluate performance of teletype-writer and data communication systems or equipment. The unit is illustrated (fig. 1-1) with its cover open and closed.

1-8. Description

a. Basically, the Pattern Generator consists of four principal sections: sign pattern generator, distortion generator, output circuits, and power supply.

(1) Signal Pattern Generator. The unit can generate the following telegraph output signal patterns:

(a) Continuous Mark or Space.

(b) Reversals-alternate Mark and Space bit in a serial stream.

(c) FOX message-a 5-level format and (strap selectable) one or two 7-levels or one 8-level format.

1 5 level (Baudot) Test Message

< ≡ ↓THE > QUICK > BROWN > FOX > JUMPS > OVER > A > LAZY > DOG> ↑↑ 123467890 ↓ TEST >

2 7-level IBM-BCD or Standard Selectic (Correspondence) Test Message

NL IL IL IL IL IL IL IL IL UC THE > QUICK > BROWN > FOX > JUMPS> OVER > A > LAZY > DOG > LC 1234567890.

3 8-Level (ASCII) Test Message

< ≡ DEL THE > QUICK > BROWN > FOX > JUMPS > OVER > A > LAZY > DOG > 1234567890 > U*U*U*U*

Symbol Legend

< Carriage return	↑(or LC)	Figures shift (lower case)
≡Line feed	NL	New line (carriage return, line feed)
>Space		
↓ (or UC) Letters shift (upper case)	IL	Idle
	DEL	Delete
BLK BLANK		

(d) All output signal patterns are start-stop and can be generated at any one of four switch-selectable baud rates (customer specified). Internal strapping options are provided to establish: ASCII, IBM-BCD or IBM Correspondence (Standard Selectric) FOX message outputs; even, odd, or no parity for 7- or 8-level codes; a 1- or 2-unit stop pulse (Mark); bit rates; 115-or 230-volt ac power input; and output signal polarity.

(2) Distortion Generator. The unit can provide output signal containing bias distortion in amounts ranging from 0 to 37.5 percent, in 12.5 per cent increments. The type of distortion introduced, switch-selectable, may be Marking bias, Spacing bias, or switched bias.

(3) Output Circuit. Pattern Generator output circuits provide two levels of signal output:

(a) Low-level logis (±6 volts) which may be internally stopped to conform with EIA standard RS-232B or MIL-STD-188B.

(b) High-level electronic relay closures for keying neutral telegraph loops.

(4) Power Supply. The dc operating voltages for the Pattern Generator are supplied by an inverter circuit which receives power from an internal, rechargeable 5-volt battery (batter operation), or from a fullwave power supply (ac operation). Recharging current is supplied to the battery when the ac line cord is connected to a 115-volt or 230-volt (strap selectable) 60Hz power source. The battery condition may be checked by means of a front-panel indicator lamp and switch.

b. The Pattern Generator is contained in a 2-piece, molded plastic carrying case provided with a fold-away handle (fig. 1-1). All operating controls and indicators, located on the top panel, are protected by a sliding aluminum cover; when open, the sliding cover permits access to the ac line cord storage compartment in the Side of the unit. Output signal connections are made at jacks on the unit's front pan; ac power and neutral loop fuses are recessed in the bottom of the unit. All Pattern Generator electronics are solid-state (including integrated circuits) and, except for the power transformer and batteries, are constructed on two printed-circuit (PC) cards (Assembly A and A2). For access to internal components for maintenance and repair, required, the upper portion of the carrying case may easily be removed.

Table 1-1. Tabulated Data

Item	Description
OUTPUT SIGNALS:	
Patterns	Reversals. Steady Mark or Steady Space. 5-level (Baudot) FOX message. One (strap selectable) 7 - or 8-level Fox message: ASCII(8-level) IBM-BCD(7-level) IBM Standard Selectric (Correspondence) (7-level)
Mode	Start-Stop.
Stop-Bit	1- or 2-unit, strap selectable for each rate.
Baud Rates	Any four customer-specified speed from 37.5 to 600 baud.
Parity	Fox 7- or 8-level codes, odd, even, or none (strap selectable).
DISTORTION:	
Types	Marking bias, Spacing bias, and switched bias (alternate Mark/Space bias on a character basis).
Amount	0, 12.5, 25, and 37.5 percent.
OUTPUT LEVELS:	
High	Solid-state closure for neural loop keying, maximum 100ma at 300 volts. (External loop batteries required). Unaffected by polarity of battery on tip/sleeve of NEUTRAL LOOP output jack.
Low	Logic-level output (±6 volts) compatible with MIL-STD-188B or EIA standard RS-232B (strap selectable).
OPERATING MODES	AC or battery.

Table 1-1. Tabulated date-Continued

Item	Description
BATTERY MODE OPERATING TIME	20 hours (approximate) continuous operation, with fully charged battery.
BATTERY CHARGING TIME	16 (approximate) from full discharge to charge condition with power off. Unit may be operated while battery is being recharged (trickle charge).
POWER REQUIREMENTS: Ac Battery	 115 or 230 (strap selectable) volts, 60 Hz. 5 volts, 85ma.
DIMENSIONS (inches)	3-13/16 wide, 11-1/2 high, 3-5/8 deep.
WEIGHT(pounds)	3-1/2

CHAPTER 2

SERVICE UPON RECEIPT AND INSTALLATION

Section I. PREPARATION FOR USE

2-1. Unpacking

a. When shipped from the factory, the Pattern Generator has all customer-specified wiring options installed so that it may be placed immediately into operation after it has been unpacked.

b Remove the Pattern Generator from its packing case, and carefully check for damage that may have occurred during shipment. Immediately notify the carrier or higher echelon of any damage to the equipment.

NOTE

Do not destroy or discard the packing case. It can be used when reshipping the unit to the manufacturer or repair facility in case of equipment damage or malfunction.

2-2. Electrical Connections

a. Use of the Pattern Generator with low-level or neutral loop circuits requires proper external connections be made to the front-panel jacks. Particular applications may require that certain customer-specified factory wired strapping connections be changed; the pattern generator contains strapping terminals for such alternate configurations to satisfy requirements of different system applications and uses. Refer to paragraph 4-6 for a description of the various strapping options.

b. Output jacks for high-level (neutral) and low-level (polar) signals are located on the unit's front panel. The output jacks to be used depend on the type of circuit being tested. Use a Western Electric plug Type 347 (or equivalent) for connections to the NEUTRAL LOOP jack; use a Pomona Type MDP dual banana plug (or equivalent for connections to the LOW LEVEL jacks.

c. The Pattern Generator provides solid-state switching for the high-level output circuit; therefore, the user must ensure that adequate current-limiting resistance is present in the external loop circuits. The high-level output circuit uses a diode-bridge configuration to permit wiring of either polarity on the tip and sleeve of the NEUTRAL LOOP telephone output jack, thus eliminating the possibility of equipment damage.

Section II. INSTALLATIONS INSTRUCTIONS

2-3. Operating the Pattern Generator

All controls and indicators used during normal operation of the Pattern Generator are located on the top pan, and output signal connections are made at the front panel (fig. 1-2). Fuses are located on the bottom of the unit.

Table 2-1. Controls, Indicators, Jacks and Fuses

Control Indicators Jack or Fuse	Function
DATA indicator lamp	Lights when Mark is generated. Functions with BAT switch to indicate condition of internal battery; when BATT switch is depressed, lamp lights if battery has more than 0.5 operating hour remaining.
PWR switch	Depression applies power to unit.
BAT switch	When depressed, functions with DATA indicator lamp to indicate battery condition; may be used with PWR switch depressed or released.
TYPE DISTORTION (BIAS) switches	
MARK	Introduces Marking bias distortion in output signal.
SPACE	Introduces Spacing bias distortion in output signal.
SW	Introduces switched bias distortion (alternate Mark/Space bias, on a character basis) in output signal.
PERCENT DISTORTION switches	
0	Introduces no distortion (0 percent) in output signal.
12.5	Introduce 12.5 percent bias distortion in output signal.
25	Introduces 25 percent bias distortion in output signal.
37.5	introduces 37.5 percent bias distortion in output signal.

Table 2-1. Controls, indicator, Jacks, and Fuses--Continued

Control, Indicator, Jack, or Fuse	Function
RATE switches (four)	Each switch indicated baud rate of reversal and FOX message output signal.
PATTERN switches: 5 LEV 8 LEV (or IBM 7 LEV) REV MARK SPACE	 Selects 5-level code (Baudot) FOX message output signal. Selects 8 -level ASCII, or 7 -level IBM-BCD or Standard Selectric (Correspondence) message output signal (established by customer-specified strap option). Selects reversal (alternate Mark and Space) output signal. (Output distortion automatically reduced to O percent if SW switch *is* also depressed.) Selects steady Mark output signal. Selects steady Space output signal.
LOW LEVEL jacks (SIG and GND)	Provides output connections for low-level (± 6-volt) output signal.
NEUTRAL LOOP phonejack	Provides output connection for high-level output signals .
F1 fuse	Fuses ac power line.
F2 fuse	Fuses high-level (neutral loop) output signal line.

2-4. Preliminary Setup

The general procedure for setting up the Pattern Gen erator, prior to operating the unit, is described below

a. Make certain that the correct internal strapping connections (paras 4-6) have been made for the given application.

b. Determine whether the mode of operation will be ac or battery.

(1) For the ac mode, connect the ac line cord to 150 or 230-.volt (as required), 60Hz power source.

(2) For battery mode, check the condition of the internal battery by depressing the BAT switch and observing the DATA indicator lamp. Use the chart below as a guide to determine whether the battery's condition will permit battery operation.

Data Indicator Lamp Light Intensity Level	Battery Condition
Dark (lamp does not light)	Completely discharge output voltage too low to operate unit.
Dim (same as when a Mark is - being generated)	Almost fully discharge; battery should be recharged.
Bright	Output voltage can operate unit for at least 0.5 hour.

2-5. Operating Procedures

After performing the preliminary setup, use the procedure outlined below as a guide for operating the Pattern Generator.

a. Select the output pattern by depressing the appropriate PATTERN switch.

NOTE

Steady Mark and Space output patterns are not affected by the RATE, PERCENT DISTORTION, and TYPE DISTORTION (BIAS) switches.

b Select the baud rate of the output pattern by depressing the desired RATE switch.

c. If distortion is to be introduced in the output pattern, select the appropriate type and amount of distortion by depressing the appropriate TYPE DISTORTION (BIAS) and PERCENT DISTORTION switches, respectively. The PERCENT DISTORTION 0 switch *must* be depressed if no distortion is to be introduced in the output pattern.

NOTE

No distortion can be introduced in the output pattern if the REV and SW switches are both depressed.

d. Turn ON the Pattern Generator by depressing the PWR switch. Check that DATA indicator lamp:

(1) goes ON if a steady Mark (positive) output pattern has been selected (If steady Space has been selected, the DATA indicator lamp should *not* go ON);

(2) blinks intermittently if 5-, 7- or 8-level, or reversals has been selected.

2-6. Interpreting Indications

After performing the operating procedures described above, the Pattern Generator will be operational for the conditions established. Changes may be made in output pattern characteristics (e.g, percent distortion, type distortion, etc.) while the unit is in operation. During long periods of battery operation, occasionally check battery condition, by means of the

BAT switch and DATA indicator lamp. There may be a momentary spike introduced in the high-level output loop when the battery is checked.

2-7. Battery Charging Procedure

When fully charge, the battery can supply power to operate the unit contiguously for approximately 20 hours. If the battery discharges completely, it can be brought to full charge in approximately 16 hours by turning OFF the unit and connecting the line cord to an ac outlet. Operation of the unit can be immediately restored even when the battery has been completely discharged by inserting the ac line cord into a power outlet. During this time, the internal battery receives a trickle charge which helps restore the battery and maintain it in a charged condition. After long periods of battery operation, it is recommended that the battery recharged to restore to a fully charged condition.

CAUTION

DO NOT permit extensive periods of discharge, or the life of the battery will be reduced. To preserve battery charge, always turn OFF power when the unit is not in use.

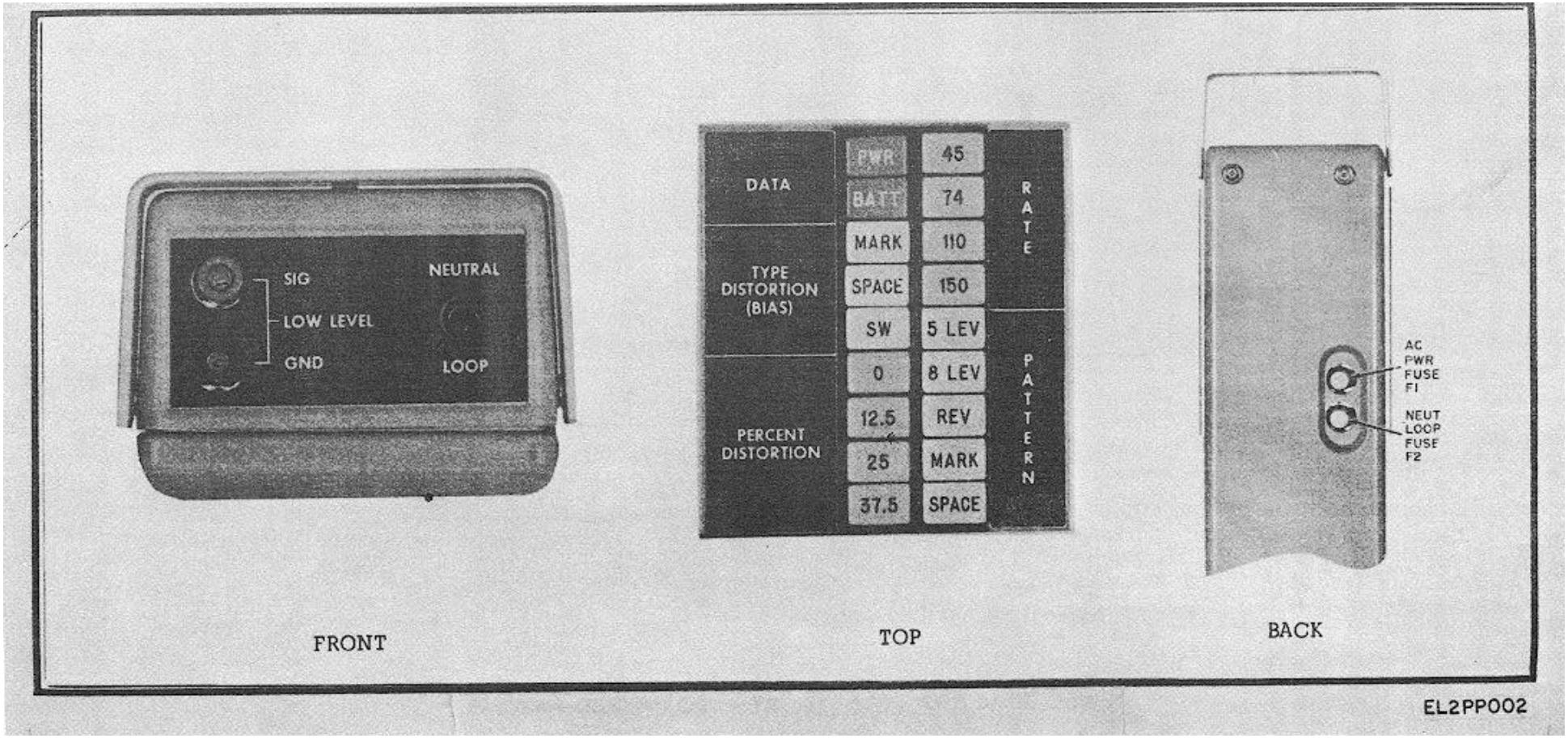

Figure 2-1. Pattern Generator--Front, Top and Back Views.

CHAPTER 3

PRINCIPLES OF OPERATION

3-1. General

Pattern Generator operation is described in the following paragraphs, on an over-all bias, using a block diagram to illustrate interrelationships of major function sections. Since most Pattern Generator circuits are unrepairable IC modules, details are provided only for circuits containing discrete components.

3-2. Overall Functional Description

The Pattern Generator block diagram (fig. 3-1) shows major functional sections, and principle control signals and data paths; power supply and switch control details are omitted, for simplification. Abbreviated sign names between functional locks are the same as those shown on the schematic diagrams provided in the Maintenance section of this manual.

3-3. Time Base Generator

The time base generator produces four frequency-stable outputs from which all timing, gating, and is distortion generating signals are derived. A free-running, RC oscillator (the basic timing device) drives a frequency countdown circuit that provides clock (CL), F1, F2, and F3 output at the correct frequencies for the selected baud rate. As show in the timing diagram (fig. 3-2), F1, F2, F3 and 1/2, 1/4, and 1/8, respectively, of the clock frequency.

a. These four output and (except for C) their complements are used by the distortion generator circuits to produce time- controllable shift pulses for the data output shift register.

b. The CL output is applied directly to the shift register for use as a left shift (LS), or parallel enter signal, after the shift register has been emptied.

3-4. Distortion Generator

Under the control of the TYPE DISTORTION and PERCENT DISTORTION switches, the distortion generator uses the four outputs from the time base generator to produce time-controllable right (se) shift (RS) pulses for the data-output shift register.

a. Distortion Selection. Bias distortion can only be introduced in the Space-to-Mark transition of the shift register data output DO, see timing diagram, fig. 3-2.

(1) When zero distortion is selected, the distortion generator produces a true" RS pulse that causes the data output Space-to-Mark (S/M) transition to occur at the proper time (for the baud-rate selected) after the Mark-to-Space (S) transition (true shift pulses are always generated for M/S transitions).

(2) If Marking bias is selected, the distortion generator produces RS pulses that cause the S*IM* transition to occur earlier than where the true shift would normally take place.

(3) For Spacing bias, the RS pulse produces a S*IM* transition at a point later than where the true shift would normally take place.

(4) Switched bias produces the same effect, alternately introducing Marking and Spacing bias, on a character-by-character basis.

(5) Percent distortion is the amount of time that the Mark bias or Space bias RS pulse is shifted in time (earlier or later) with respect to the true-shift point.

b. Circuit Operation. The shift control circuit in the distortion generator assures that RS pulses, whether true shift or distortion (true) shift, occur at the proper intervals for the selected baud-rate.

(1) This circuit receives two inputs: (1) a pulse produced by ANDing CL, F1, F2, and (2) a bias select (BS from the shift register. As shown in the timing diagram (fig. 3-2) the CL, F1, F2 F3 pulse is generated whenever a transition (MS or S*M)*is to occur in the data output; the BS input is the next-to last bit in the data output shift register. Thus, by sensing each transition and determining whether the next pulse to be shifted out on the line is to be a M/S or an S/M transition, the circuit can generate a true-shift or trueshift output. True-shift outputs, which always occur on M/S transitions or when zero distortion has been selected, are coupled directly through a shift pulse selected circuit to the RS input of the shift register. Trueshift outputs, produced by S*IM* transitions when other than zero distortion has been selected, are applied as an enabling input to a Mark/Space bias generator.

(2) The type and amount of distortion provided are controlled by the Mark/Space bias generator circuit which functions only if a true-*sh*ift input is present, indicating that a SM transition containing some value of distortion is to occur. Once enabled, the circuit may produce Mark bias or Space bias, depending on the selected TYPE DISTORTION switch. If the MARK switch is depressed, the Mark bias generator is

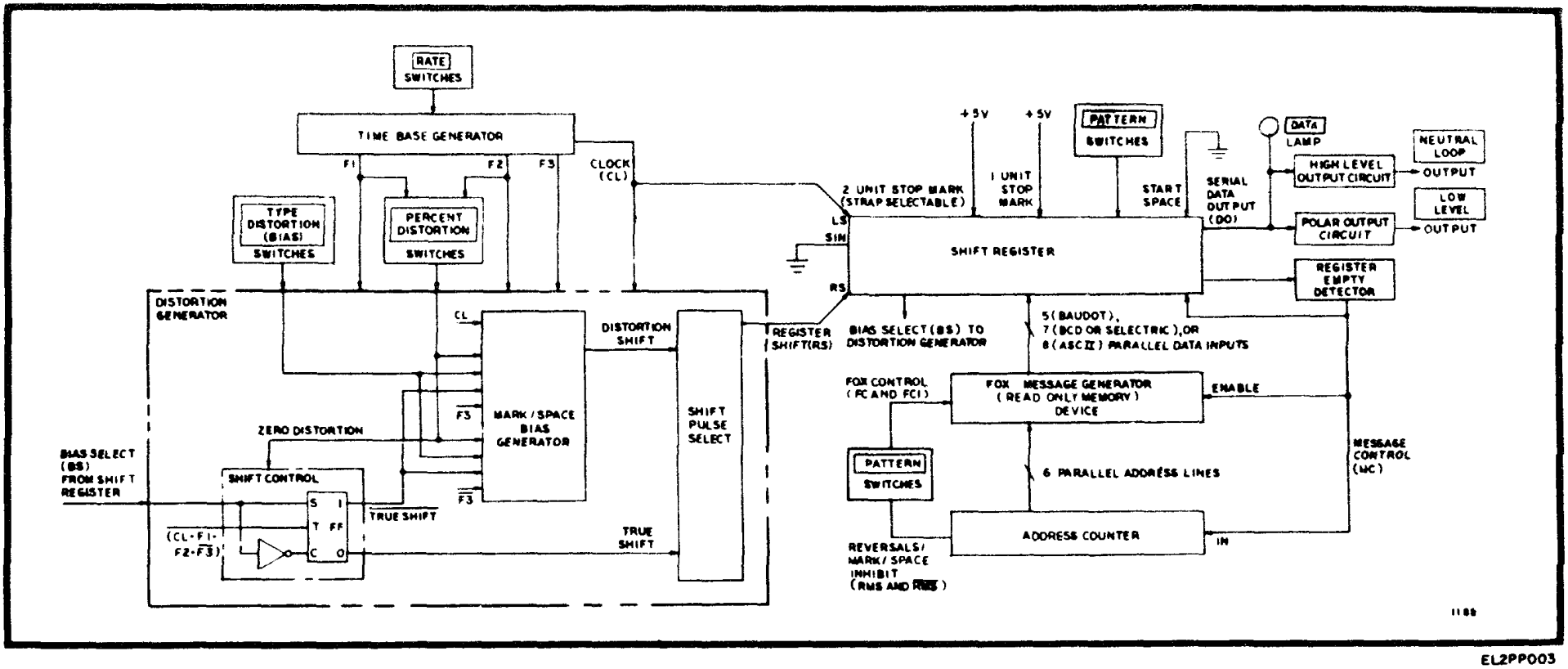

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Figure 3-1. Pattern Generator, Block Diagram.

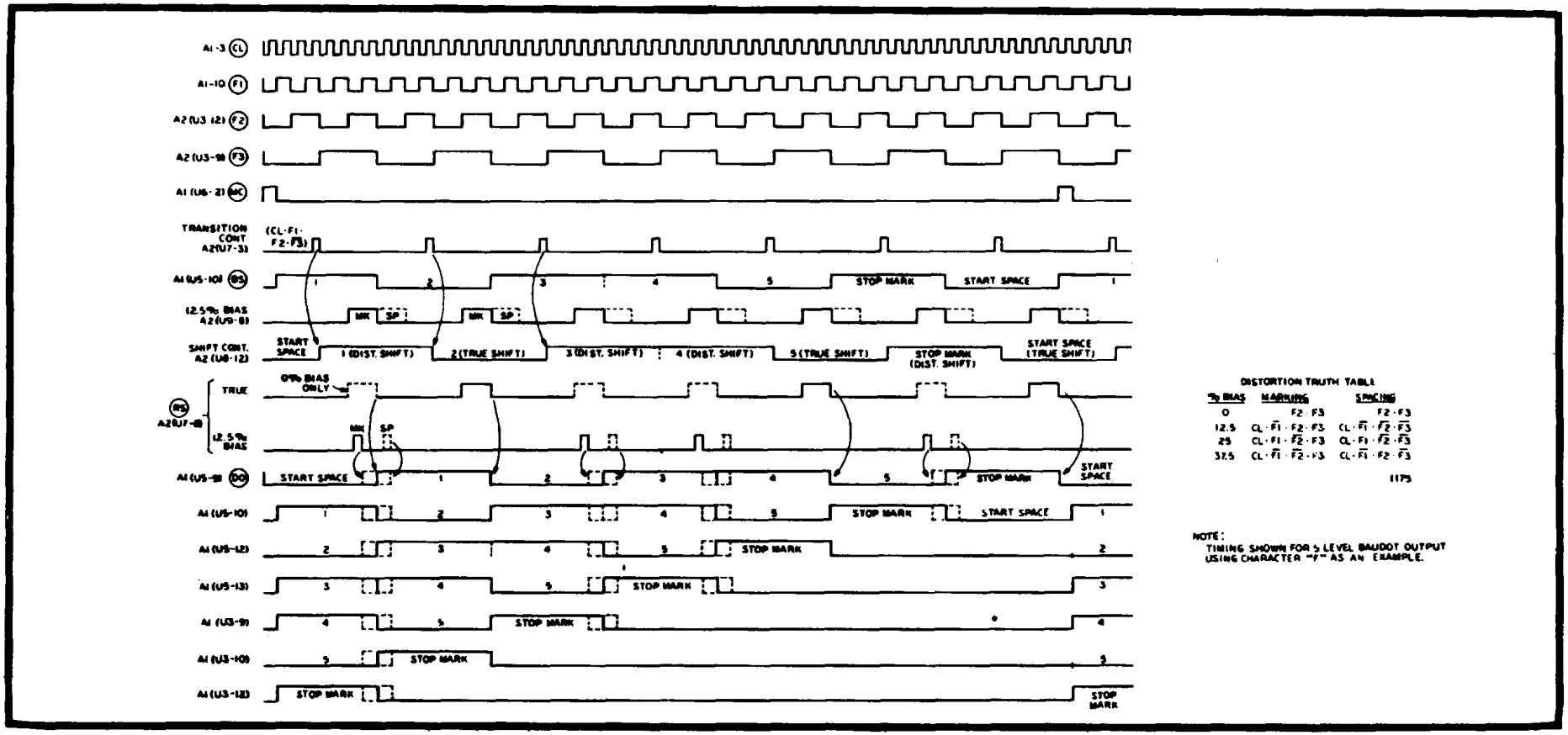


Figure 3-2. Pattern Generator, Timing Diagram

enabled and the space bias generator is disabled (the reverse is true if Spacing bias is selected). For switched bias
operation, a flipflop alternately enables and disables each circuit on a character-by-character basis.

(3) The amount of distortion produced is established by the PERCENT DISTORTION switch selected. Except for zero distortion, each switch provides various combinations of F1 and F2 input (as well as their complements) to the Mark/Space bias generator where they are combined with F3 (Marking spacing only), F3 (Spacing only), and CL to produce time variable distortion shift pulses. The truth table on the timing diagram lists various CL, Fl, F2, F3 combinations that produce the desired percent distortion; examples of 12.5 per cent Mark and Space bias RS pulses are also shown on the timing diagram. Selecting higher distortion values displays the Mark or Space bias RS pulses further in time from the point where a true shift (zero bias) normally take place.

(4) Distortion shift output pulses from the Mark/Space bias generator, or true-shift output pulses from the shift control circuit, are applied as RS inputs to the shift register via a shift pulse select circuit. This circuit provides a simple OR function, by gating through whichever signal is present. Both signal cannot be present at the same time since the two conditions for establishing true or distortion shift are logical opposites (M/S or S/M transition of next-to last bit in the shift register, and selection of bias or no bias).

3-5. Address Counter

A 6-stage, ripple through, binary counter, this circuit controls operation of the FOX message generator whenever a 5-level, 7-level, or 8-level pattern is selected (it is inhibited by RMS and RMS input from the PATTERN switches, when steady Mark, steady Space, or reversals output is output is selected). With the inhibit removed, the address counter is advanced from a count of 0 to 63, by message control (MC) clock inputs from the shift register. A clock input is presented each time the shift register is emptied, indicating that the latter is ready to accept the next character, in parallel input form, from the FOX message generator, at which time the MC input advances the circuit count by 1 and the new output address is applied to the FOX message generator via six parallel lines. When the maximum count of 63 is reached, the counter automatically restarts at O.

3-6. Fox Message Generator

A preprogrammed, read-only memory device, this circuit provides five (for Baudot, seven (for IBM-BCD or Standard Selectric, or eight (for ASCII parallel data- bits to the data output shift register for generation of Fox messages. The programmed outputs are controlled by the 6-bit parallel address input supplied from the address counter, and two additional inputs provided via the 8-LEV (or IBM 7-LEV) and 5-LEV PATTERN switches.

a. Binary input required to generate the various preprogrammed FOX message output (par 1-8) are defined below.

Binary Input	Code
0-63	Standard selectric (7-level)
64-127	IBM-BCD(7-level)
128-191	BAUDOT(5-level)
192-255	ASCII(8-level)

b. Since the six address input lines cannot provide a binary count greater than 63, two additional input (FC and FC1, representing the seventh and eighth binary digits [64 and 128, respectively]) are supplied from the 8-LEV (or IBM 7-LEV) and 5-LEV PATTERN switches so that the FOX message generator produces output codes other than standard Selectric.

(1) for IBM-BCD operation, line FC is enabled; the count thus starts at 64 and is advanced from 64 to 127 by the six address input lines.

(2) For Baudot operation, line FC1 is enabled; the count, which starts at 128, is advanced to 191 by the six lines.

(3) In ASCII operation, FC and FC1 are both enabled (128+ 64), so that the count starts at 192 and is run to 255.

NOTE

Baudot FOX messages are always generated when the 5-LEV push-button is depressed. However, only one of the three other (7- or 8-level codes is generated when the applicable push-button is *de*pressed, as determined by customer-specified strapping option.

c. To conserve power, the FOX message generator is enabled only when the shift register has been emptied and is therefore ready for the next parallel entry. This is effected by suing the MC pulse, present only when the shift register is empty, to enable FOX message generator operation which then parallel-load the shift register; once the register is loaded, the MC pulse is removed and the FOX message generator disabled until all the data-bits have been shifted out. Serial data output (DO) from the hit register are simultaneously applied to high-level and polar output circuits. A top panel mounted DATA lamp in the data output circuit lights when the output bit is a Mark (positive).

3-7. Shift Register

Comprising three IC circuits, the 11-stage shift register performs a parallel-to-serial conversion of the message characters supplied from the FOX message generator. The start-space bit, and a 1-unit StopMark bit, and a strappable 2-unit stopMark bit are hard-

wired to the shift register. Only the five Baudot, seven IBM-BCD or Standard Selectric, or eight ASCII data bit are supplied from the FOX message generator Operation of the shift register with 5-, 7-, or 8-level inputs-as well as steady Mark, steady Space, or reversals-is controlled by the applicable PATTERN switches.

a. In 5-, 7-, or 8-level operation, shifting the last bit of a character onto the data output line is sensed by a register empty detector, which then supplies an MC pulse to the address counter and FOX message generator

(1). This pulse (1) enables generation of the next FOX message character, and (2) is fed back to the shift register where, with the LS (clock) input from the time base generator, it enables entry of the next set of parallel data-bits into the shift register. Shift pulse from the distortion generator then shift the hard wired Space serial input (Sin) through the register as data-bits are transferred onto the data output line This process continues until the last (stop-Mark) data bit is shifted out (register empty and an MC pulse is generated to repeat the entire procedure.

(2) A BS output, representing the next-to-last bit in the shift register, causes the distortion generator produce true-shift or distortion-shift output as described previously.

b. During 8-level operation, all three IC circuits in the shift register are used. For 5-level operation, the three stages of the second IC circuit are bypass (through operation of the 5-LEV push-button) so that only the first and last IC circuits are used. In the 7-level mode, a strap option serves to bypass one stage of the second IC circuit.

c. For steady Mark, Space, or reversals operation only one of the three shift register ICs (that containing the last four stages) is used, and the selected PATTERN switch provides the proper input.

(1) For steady Mark or Space, the positive voltage or the ground (respectively) applied to the IC signal input is continuously shifted through the last four stage of the register.

(2) For reversals, an inverter between the fourth stage output and the signal input to the IC cause Mark and Space signals to be shifted through the register's last four stages in an alternating pattern.

3-8. Output Circuits

The Pattern Generator includes a high-level (neutral loop) output circuit and a low-level (polar) output circuit. Both circuits comprise discrete components and provide outputs via jacks on the units front panel. ‘

a. The high-level output circuit consists of a buffer amplifier, and a fuse-protected keying transistor connected to the NEUTRAL LOOP output jack through a full-wave diode bridge. The full--wave bridge permits either polarity of the external loop to be connected to the tip or sleeve of the NEUTRAL LOOP jack, without damaging the output keying transistor.

b. Low-level (± 6 volts) output are supplied from a 3-transistor polar keying circuit that performs current-limiting ad has a low-impedance output. The common-emitter output of the circuit is connected to the LOW LEVEL SIG jack, and the return line is connected to the LOW LEVEL-GND jack.

3-9. Polar Output Circuit (See fig. FO-1 for schematic diagram)

Serial data is applied to the polar output circuit through pin 10 of inverter U6.

a. When a Mark (positive) signal appears at pin 11 of inverter U6, the output at pin 10 is grounded so that Zener diode VR4, a 13 volt regular, does not conduct; the Q4 base is held at - 10 volts, keeping Q4 cut off. Thus the current flow through diodes CR16 and CR19 forward-biases Zener diode VR5, cutting off Q5 and driving Q3 into saturation-to supply a ±6-volt output at the LOW LEVEL SIG jack.

b. With a Space signal (ground at U6-11, output at pin 10 rises to +10 volts. With sufficient reverse breakdown voltage, the 13 volt drop across VR4 drives Q4 into conduction-applying a potential of approximately -7 volts at the Q5 base and approximately -6 volts at the Q3 base. This cuts off Q3 and drives Q5 into saturation-producing a -6-volt output at the LOW LEVEL-SIG jack.

c. Diodes CR17 and CR18 serve as current-limits for Q3 and Q5, respectively. Under normal operating conditions, CR 17 and CR18 do not conduct However, when the Q3 or Q4 emitter approaches a short-circuit condition, the associated diode conducts, biasing the transistor toward cutoff.

3-10. Power Supply Inverter (see fig. FO-1 for schematic diagram)

This circuit, which receives a 5-volt dc input from the battery, supplies +10- and -10-volt dc outputs for various circuits on Pattern Generator assemblies A1 and A2. Battery input is applied to astable multivibrator Q1-Q2, which generates a 4 to 5kHz squarewave having a peak-to-peak amplitude of approximately 20 volts. This squarewave is coupled through transformer T1 to bid rectifier CR12-CR15, resulting in + 10- and -10-volt dc outputs (from opposite sides of the bridge rectifier) that are filtered by capacitors C4 through C7.

3-11. High-Level Output Circuit see fig. FO-2 for schematic diagram)

Serial data is applied, via buffer Q2, to the high-level output circuit comprising keying transistor Q1 and bridge rectifier CR3-CR6. With BATT switch S2 re

leased, signals from Q2 are applied to Q1 through DATA lamp DS1; with the switch depressed, signals are applied from Q2 to Q1 through R39.

a. Keying transistor Q1 is connected to the tip and sleeve of NEUTRAL LOOP jack J, through fuse F2 (which provides overload protection for Q1) and diode bridge CR3-CR6 (which permits the external loop, using either polarity, to be connected to the NEUTRAL LOOP jack without damaging the keying transistor).

b. When a Mark (positive) signal is applied, Q1 conducts. If the external loop is connected + to - on the tip and sleeve, respectively, of the NEUTRAL LOOP jack, current flows through CR5, F2, Q1, and CR4. If the polarity is reversed, current flows through CR3, F2, Q1, CR4. When a Space signal is applied, Q1 is cut off, opening the external loop.

3-12. Battery Test Circuit (see fig. FO-2 for schematic diagram)

The battery test circuit comprises transistor Q3, BATT switch S2, and DATA lamp DS1.

a. When BATT switch S2 is depressed, the 5-volt battery: (1) provides collector voltage for Q3 through BATT lamp DS1; and (2) is connected across 4.3-volt Zener diode VR1 and resistor R32 in the Q3 base circuit. If battery voltage exceeds 4.3 volts, VR1 conducts and the resultant voltage drop across R22 turns ON Q3, causing the DATA lamp to light. The higher the charge condition of the battery, the more heavily Q3 conducts, increasing the intensity of DATA lamp brightness.

b. If the battery is excessively discharged so that its voltage does not exceed the VR1 breakdown voltage, Q3 is cut off and the DATA lamp is not lighted.

c. Fuse F3, connected in series with the battery across the 5 volts dc input (see fig. 4-1 for schematic drawing), is provided as a safety precaution to protect the battery in the event of an overload (short circuit) condition.

CHAPTER 4
MAINTENANCE INSTRUCTIONS

4-1. Maintenance Practices

Except for replacement of the battery and fuses, it is recommended that the Pattern Generator be returned to the factory for service. Where field service is necessary, it should be performed only by an engineer or technician thoroughly familiar with operation of the unit and experienced with similar equipment. The performance test described in paragraph 4-3 can serve to establish the unit's general operation condition. If the unit malfunctions, signal trace using the waveforms shown in figure 3-2 and the diagrams provided in figures 4-1, FO-1, and FO-2. Perform the frequency adjustments as required, as described in paragraph 4-5. To select parity mode, stop-Mark width, baud-rate, output phase, 7- or 8-level code, and ac power input other than those factory-strapped, proceed as described in paragraph 4-6.

a. Battery Re*placemen*t. If the battery cannot be brought up to a fully charged condition as described in paragraph 2-7, replace the battery as described below.

(1) Remove the three screws (two near the carrying handle hinges, and one at rear of unit) that fasten top of Pattern Generator case to bottom of unit.

(2) Lift cover off unit, gently rocking cover back and forth, making sure not to force cover against DATA lamp or pushbuttons in top of unit or output jacks in front of unit

(3) Remove battery from holder.

(4) Remove red plastic caps from each end of battery.

(5) Unsolder wire from terminal on each end of battery, and solder wires to replacement battery (black to negative, white to positive).

(6) Replace plastic caps on battery.

(7) Replace battery in holder, being careful not to pinch wires.

(8) Carefully replace top cover, front first, making sure that the DATA lamp come through hole in cover.

(9) Replace and tighten three securing screws.

b. Fuse Replacement. To replace the ac input or neutral loop fuses (bottom of the unit, see fig. 1-2), unscrew the fuse-cap and extract the fuse (fuse is equipped with two pin that plug into holder). Insert new 0.1- ampere fuse, and replace cap. To replace battery fuse F3 (see fig. 4-4) proceed as follow

(1) Remove the three screws (two near the carrying handle hinge, and one at rear of unit) that fasten top of Pattern Generator case to bottom of unit.

(2) Lift cover off unit, gently rocking over back and forth, making sure not to force cover against DATA lamp or pushbuttons in top of unit or output jacks in front of unit.

(3) Remove four screws that fasten bottom cover of Pattern Generator and remove cover.

(4) Remove fuse, located under battery holder bracket, and insert new 1 ampere fuse.

(5) Replace and tighten bottom cover with four *se*curing screws.

(6) Carefully replace top cover, front first, making sure that the DATA lamp comes through hole in cover.

(7) Replace and tighten the three securing screws.

4-2. Test Equipment Required

The test equipment listed below is required for maintenance of the Pattern Generator. Manufacturer and model recommendations are typical; equivalent types may be substituted. The Common Name column specifies the name by which each test equipment is subsequently referred to.

Table 4-1. Test Equipment Required

Name	Common Name	Function
Electronic Frequency Counter, Hewlett-Pack Model HP, 5211A or	Counter	Measurement of time-base Frequencies and equivalent rates
Oscilloscope , Tektronix Model 535, or equivalent	Oscilloscope	Waveform observation and measurement. Also used for signal tracing
Multimeter, Simpson Model 2, or equivalent	Multimeter	General voltage and resistance measurements.
Data Measuring Set, STELMA Model DMS-303A, or equivalent	DMS-303A	Measurement of telegraph distortion.
teletype Printer Units (two require: 5-level code and 8-level code machines)	Teleprinter	Provide printed readout of 5- or 8-level FOX test messages for verification of equipment ac curacy.

Table 4-1. Test Equipment Required-Continued

Name	Common Name	Function
Data Terminal, IBM Model 2741, or equivalent	Data terminal	Provide printed readout of 7-level FOX test messages for verification of equipment accuracy

4-3. Performance Test

Since no one combination of control settings will provide a comprehensive test of the Pattern Generator, a thorough Performance Test requires that the various functional sections of the unit be tested and evaluated separately. The performance test outlined below is designed to check the unit in a logical series of separate tests; successful completion of the test verifies equipment operation capability and can serve to define trouble symptoms.

Table 4-2. Performance Test Table

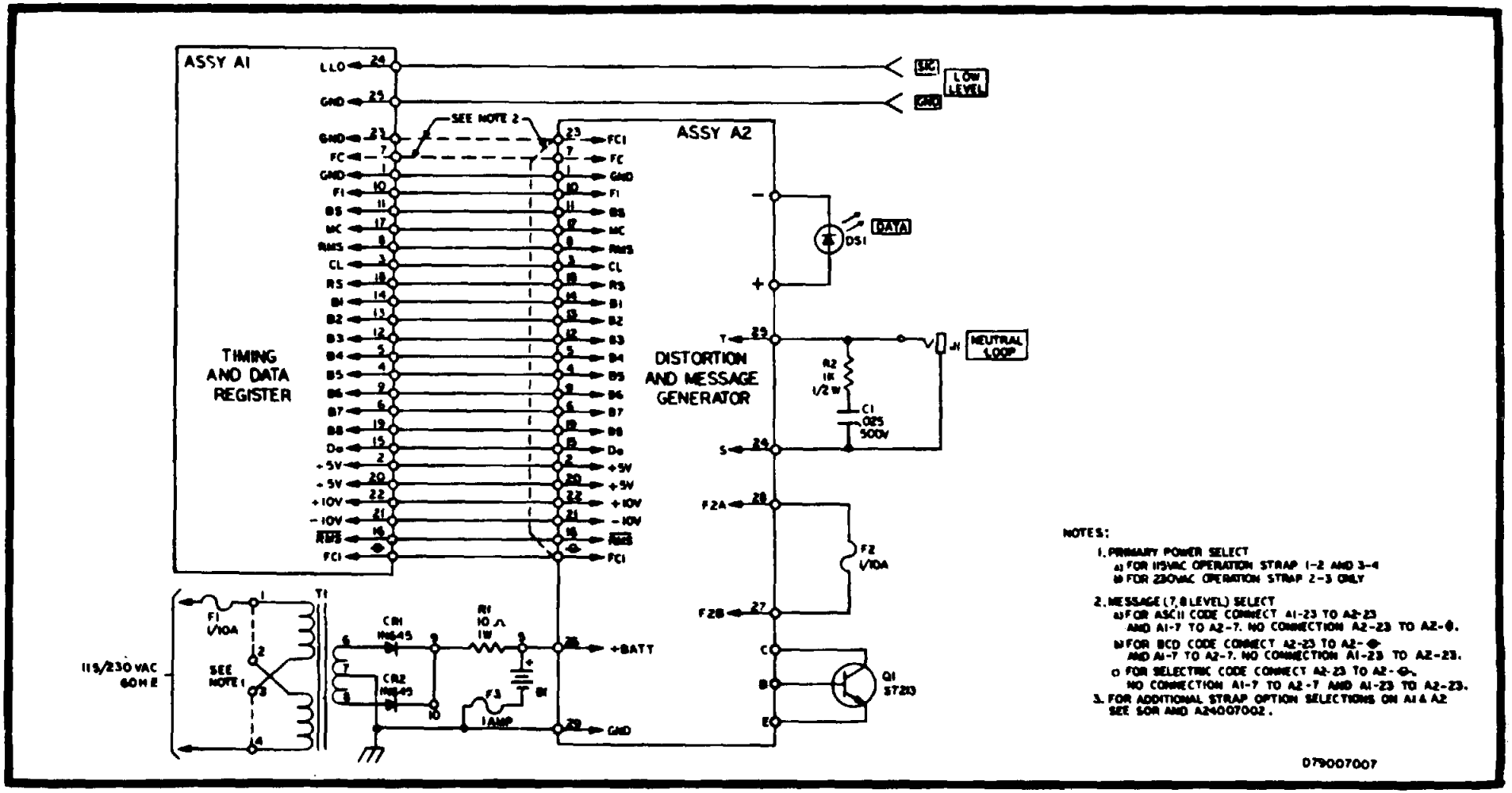
Procedure	Normal Indication
BATTERY TEST	
1. Depress BATT switch.	
2. Observe DATA lamp.	DATA lamp glows brightly. If it does not, recharge battery for several hours before continuing tests.
3. Depress and release BAT switch.	
NOTE **Continue remainder of test, with power cord plugged into ac outlet.**	
BAUD RATE TEST	
1. connect counter to LOW LEVEL jacks.	
2. Depress PERCENT DISTORTION - 0 switch.	
3. Depress PATTERN-REV switch.	
4. Depress PWR switch.	
5. Depress RATE switch in sequence, and measure output frequency on counter after each switch is depressed .	The frequencies measured by counter are one half the baud-rate values marked on RATE switches. DATA lamp blinks at selected baud-rate.
OUTPUT CIRCUITS AND PATTERN TEST	
1. Depress PERCENT DISTORTION - 0 switch.	
2. Depress PATTERN-MARK switch.	DATA lamp goes ON.
3. Measure voltage at LOW LEVEL jacks with multimeter or oscilloscope.	Test equipment indicates a steady + 6 volts if output phase is strapped for positive MARK, or a steady -6 volts if output phase is strapped for negative Mark.
4. Depress PATTERN-SPACE switch.	DATA lamp goes OFF.
5. Repeat step 3, above.	Test equipment indicates a steady - 6 volts if output phase is strapped for positive Mark, or a steady +6 volts if output phase is strapped for negative Mark.
6. Depress any RATE switch.	
7. Depress PATTERN-REV switch.	
8. Connect oscilloscope to LOW LEVEL jacks, and observe wave shape of displayed signals.	Oscilloscope displays a square wave having a peak-to-peak amplitude of 12 volts (- 6 volts to + 6 volts) with pulse-widths corresponding to value selected by RATE switch (i.e., 1/baud-rate = pulse-width).
9. Release PWR switch.	
10. Connect NEUTRAL LOOP output jack to 5-level Baudot teleprinter.	
NOTE **External loop battery and loop-limiting resistor must be provide.**	
11. Depress PATTERN -5 LEV switch.	
12. Depress PWR switch.	
13. Turn ON power to the teleprinter, and observe printout	Teleprinter repeatedly prints 5-level Baudot FOX message (see pars 1-8a(1)(c) 1 for 5-level FOX message format).
14. Depress PWR switch, turn OFF power to teleprinter, and disconnect plug from NEUTRAL LOOP jack.	
15. Reverse loop-polarity connection, and repeat steps 10 through 14.	
NOTE **Steps 16 through 21, steps 22 through 26, and steps 27 through 31 serve to check Pattern Generator performance in producing ASCII, IMB-BCD, or Standard Selectric FOX message codes, respectively. Use only the applicable steps for the Pattern Generator under test.**	

Table 4-2. Performance Test Table--Continued

Procedure	Normal Indication
16 .Connect NEUTRAL LOOP jack to 8-*l*evel ASCH teleprinter. **NOTE** **External loop battery and looplimiting resistor must be provided.** 17. Depress PATTERN-8 LEV switch. 18. Depress PWR switch. 19. Turn ON power to teleprinter, and observe printout. 20. Depress PWR switch, turn OFF power to teleprinter, and disconnect plug from NEUTRAL LOOP jack. 21. Reverse loop-polarity connection, and repeat steps 16 through 20. 22. Connect LOW LEVEL output jacks to suitable data terminal using IBM-BCD code. 23. Depress PATTERN-IBM 7 LEV switch. 24. Depress PWR switch. 25. Turn ON power to data terminal teleprinter, and observe printout. 26. Depress PWR switch, turn OFF power to data terminal teleprinter, and disconnect plugs from LOW LEVEL jacks. 27. Connect LOW LEVEL output jacks to suitable data terminal using Standard Selectric code. 28. Depress PATTERN-IBM 7-LEV switch. 29. Depress PWR switch. 30. Turn ON power to data terminal teleprinter, and observe printout. 31. Depress PWR switch, turn OFF power to data terminal teleprinter, and disconnect plugs from LOW LEVEL jacks.	Teleprinter repeatedly prints 8-level ASCII FOX message (see para 1-8a(1)*(c)3* for 8-level FOX message format). Teleprinter repeatedly prints 7-level IBM-BCD FOX message (see para 1-8a(1)*(c)2* for 7-level IBM-BCD FOX message format). Teleprinter repeated prints 7-level Standard Selectric FOX message (see para 1-8a(1)*(c)2* for 7-level Standard Selectric FOX message format).
DISTORTION TEST 1. Connect DMS-303A to LOW LEVEL jack Adjust DMS-303A controls for measurement of Marking bias on a low-level start-stop signal. 2. Depress TYPE DISTORTION (BIAS) -MARK switch. 3. Depress PERCENT DISTORTION - 0 switch. 4. Depress PATTERN- 5 LEV switch. 5. Depress PWR switch. 6. Turn ON power to DMS-303A, and measure Marking bias. 7. Depress PERCENT DISTORTION-12.5, -25, and -37.5 switches, sequence, and measure Marking bias after each switch is depressed 8. Use same general procedure described above for measuring Spacing bias and switched bias using TYPE DISTORTION(BIAS)-SPACE and-SW switches, respectively.	DMS-303A indicates 0 distortion. Distortion indicated on DMS-303A is within 3 per cent of selected PERCENT distortion switch. Distortion indicated on DMS-303A same as for Marking bias measurements.

4-4. Repair

Repair and replacement of Pattern Generator components may be accomplished using standard techniques and practices, including precautionary measures required when replacing semiconductors and integrated circuit. Parts location diagrams for components mounted on PC-cards A1 and A2 are shown in figures 4-2 and 4-3; locations of components not mounted on the PC-cards and not otherwise identified by front panel nomenclature are shown in figure 4-4. In most cases, component replacement will not necessitate recalibration or readjustment of the unit, if an exact replacement part has been used. However, if any parts in the time base oscillator on PC-card A1 are replaced, perform the adjustment procedure provided below to check for proper output frequencies.



EL2PP007

Figure 4-1. Pattern Generator, Wiring Diagram.

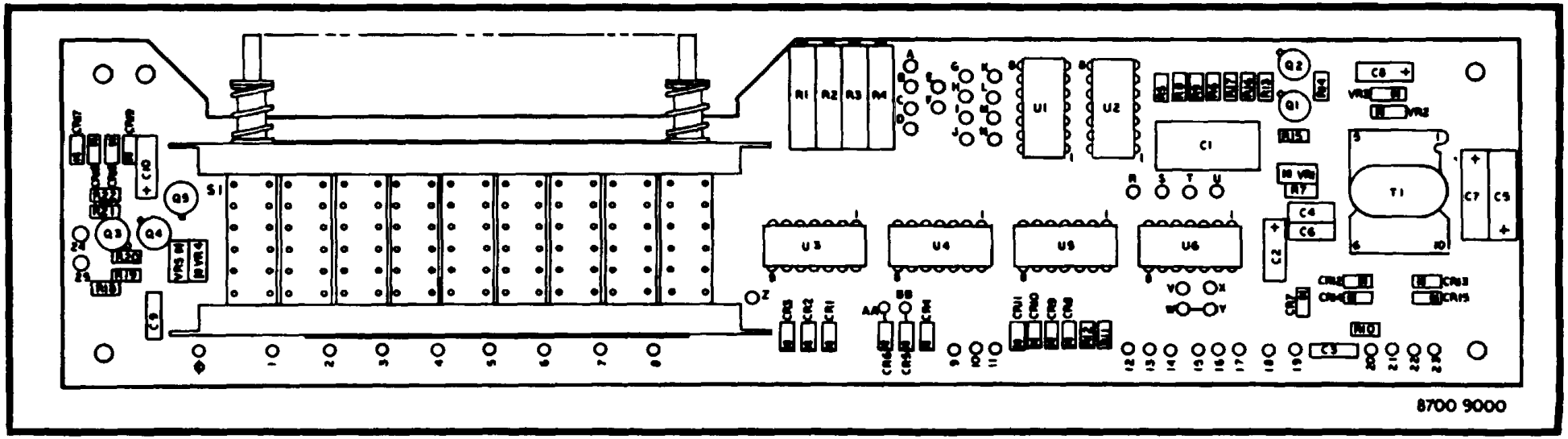


Figure 4-2. Timing and Data Register Assembly A1, Component Location Diagram.

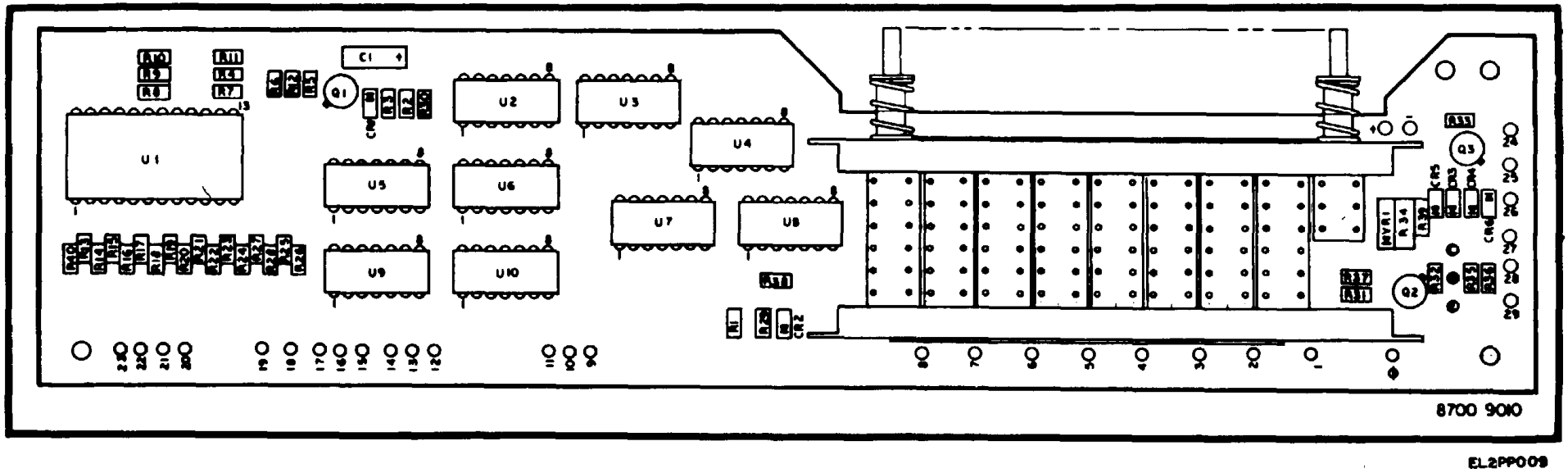


Figure 4-3. Distortion and Message Generator Assembly A-2, Component Location Diagram.

4-5. Time Base Oscillator Frequency Adjustment

The time base oscillator output frequency should be checked or adjusted whenever an oscillator-circuit component is replaced or an incorrect baud-rate output is suspected. Take all frequency measurements with the frequency counter connected to strapping terminal.

Baud-Rate	Frequency (HZ) (Meas. At Term. A1-K)
37.5	2400
40	2560
45	2912
50	3200
56	3637
61	3913
66	4267
70	4480
74	4749
75	4800
82	2400
96	3072

*Refer to RATE switch location for corresponding adjustment control.

RATE Switch Location	*Adjustment Control*
Upper	A1R1
Upper-Middle	A1R2
Lower-Middle	A1R3
Lower	A1R4

4-6. Strapping Options

Although the Pattern Generator is shipped from the factory with all customer-specified strappings options included, these options may be changed in the field to satisfy requirements of different applications and uses. PC-card A1 has strapping options to establish parity mode, stop-Mark width, output phase, baud-rates, and ac power input; strapping options may also be made between PC-cards A1 and A2 to select the desired 8-level code (ASCII) or 7-level code (IBM-BCD, or Standard Selectric). The strapping connections required to obtain the desired characteristics of these various options are described below. Refer to figures 4-2 and 4-5 for location of strapping terminals on PC-card A1.

a. Parity Mode. Strapping options provide a choice of odd parity, even parity, or no parity bit for the 7- or 8-level FOX test message characters; when no parity is selected, the particular bit-position will always contain a Mark. Strapping connections for the parity mode options are as follows:

(1) For odd parity, strap terminal T to U.
(2) For even parity, strap terminal T to S.
(3) For no parity, strap terminal T to R.

b. Stop-Mark Width. Strapping terminals are provided for each RATE switch so that a 1-unit or 2-unit stop-mark can be programmed in the FOX test messages at the selected baud-rate. Strap connections for stop-K on PC-card A1 (see fig. 4-2; the appropriate frequency for each baud-rate is listed below (if the frequency for a selected baud-rate is not as specified, adjust the appropriate control to obtain the proper frequency-see fig. 4-4 for locations of adjustment controls A1R1-A1R4).

Baud-Rate	Frequency (HZ) (Meas. At Term.A1-K)
100	3200
105	3360
110	3520
135	4304
148	4752
150	4800
192	3072
200	3200
300	4800
400	3200
600	4800

Mark width options are charted below for the various RATE switches.

Stop-Mark Width	Connect Terminal:	RATE Switch Position
1 Unit	A to F	Upper
2 Unit	A to E	
1 Unit	B to F	Upper-middle
2 Unit	B to E	
1 Unit	C to F	Lower-middle
2 Unit	C to E	
1 Unit	D to F	Lower
2 Unit	D to E	

c. Output Phase. These strapping terminals provide a means of establishing the Marking polarity (positive Mark or negative Mark) of low-level output signals. Strapping connections for the output phase options are as follows:

(1) For positive (+6 volt) low-level Mark, strap terminal X to W.

(2) For negative (-6 volt) low-level Mark, strap terminal X to V.

d. Baud Rate. Strapping is provided to select the baud-rate range of the four RATE switches. Each RATE switch may be strapped to cover one of four baud-rate ranges: 37.5 to 75, 75 to 150, 150 to 300,

and 300 to 600. In addition, a baud-rate conversion it must be ordered from Data Products , STELMA Telecommunications. This kit contains the proper value for resistors R23 through R26 to obtain the desired baud rate, and a push-button with the corresponding baud rate marking. Strapping connections for selecting baud-rate ranges and conversion kit has part numbers are charted below. After the conversion kit has been installed and the strapping has been accomplished, make fine frequency adjustment as described in paragraph 4-5.

RATE Switch Position	Baud-Rate Range	Strap Terminal:
Upper	37.5-75	G to N
	75 -150	G to M
	150 -300	G to L
	300-600	G to K
Upper-middle	37.-75	H to N
	75 -150	H to M
	150 -300	H to L
	300 -600	H to K
Lower-middle	37.5-75	I to N
	75 -150	I to M
	150 -300	I to L
	300 -600	I to K
Lower	37.5-75	J to N
	75 -150	J to M
	150 -300	J to L
	300 -600	J to K

Baud-Rate	Conversion Kit Part No. 24007002	. Baud-Rate	Conversion Kit Part No. 24007002	Baud-Rate	Conversion Kit Part No 24007002
37.5	-000	56	-007	105	-015
45	-001	61	-008	135	-016
74	-02	66	-009	148	-017
110	-003	70	-010	192	-018
150	-004	75	-011	200	-019
40	-005	82	-012	300	-020
50	-006	96	-013	400	-021
		100	-014	600	-022

e. 7- OR 8-Level Fox Message. In addition to the 5-level(Baudot) FOX Message, the Pattern Generator can also output ether one of two 7-level coded FOX messages (IBM-BCD or Standard Selectric) or an 8-level ASCII coded FOX message. Strapping connections for selecting the desired 7- or 8-level code are charted below.

ASCII		IBM-BCD		Standard Selectric	
From	To	From	To	From	To
A1-23	A2-23	A2-23	A2-0	A2-23	A2-0
A1-7	A2-7	A1-7	A2-7	NO. CONN.(A-1-7 to A2-7)	
A1-AA	A1-Z	A1-BB	A1-Z	A1-BB	A1-Z

f. AC Power Input. The Pattern Generator can operate with either a 115- or 230-volt ac input, depending on power transformer T1 strapping; see fig. 4-4. To operate from:

(1) 115 volts, strap T1 terminals 1 to 2, and 3 to 4.

(2) 230 volts, strap T1 terminals 2 to 3.

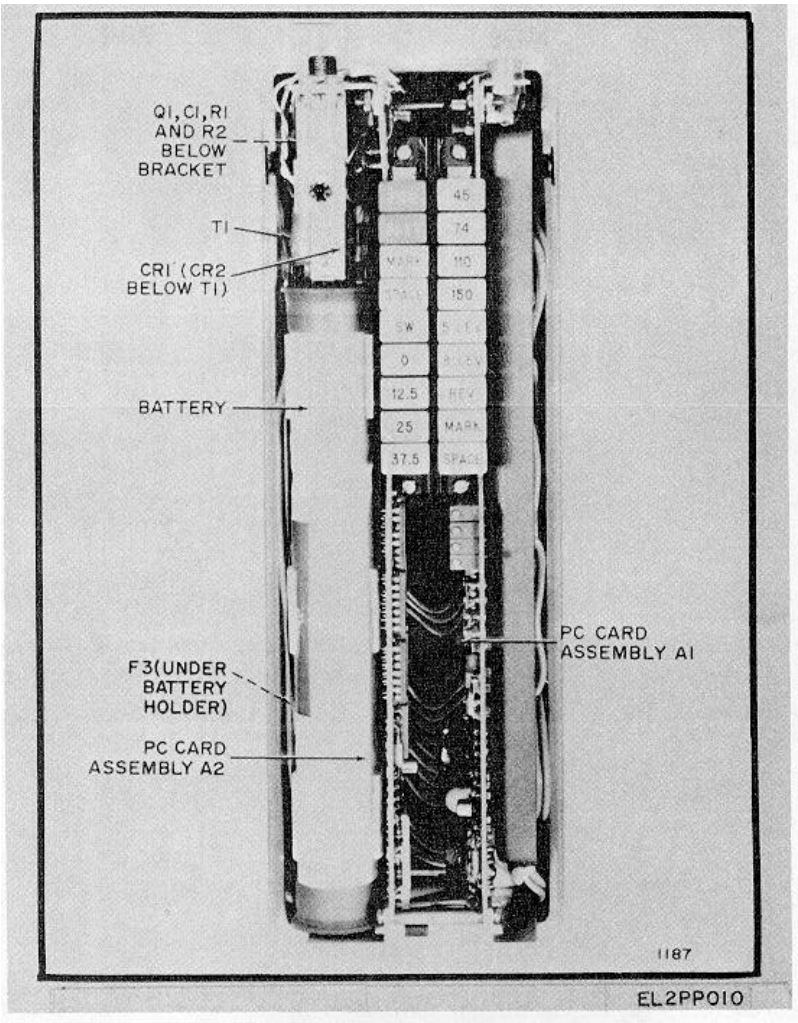


Figure 4-4. Pattern Generator, Top View, Component Location.

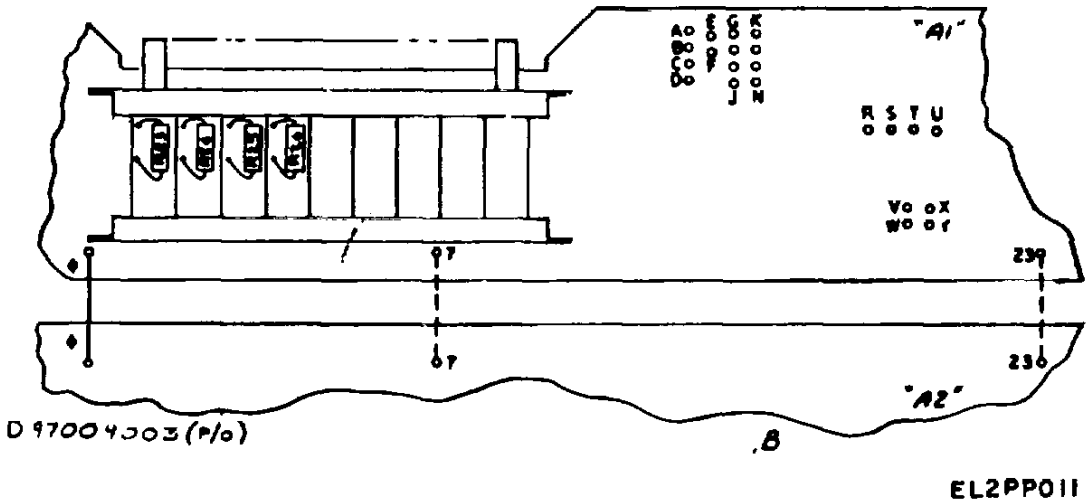


Figure 4-5. Location of Strapping Terminals and Resistor R23 Through R26 Assembly.

APPENDIX A

REFERENCES

DA Pam 310-4	Index of Technical Publications: Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA Pam 310-7	US Army Equipment Index of Modification Work orders.
TM 38-750	The Amy Maintenance Management Stem (TAMMS).
TM 7-244-2	Procedure for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX D

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

D-1. General

This appendix provides a summary of the maintenance operations for the PG-404. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

D-2. Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristic of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by brining into proper or exact position, or by setting the operation characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipment used in precision measurement. Consists of comparisons of two instrument, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part , module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

I. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remaining, or resurfacing to restore serviceability to an item by correcting specific damage, fault malfunction, or failure in a part, subassembly, mode (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/ action) necessary to restore an item to a completely serviceable operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance permitted by the Army. Overhaul does not normally turn an item like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours , miles, etc.) considered in classifying Army equipment's/components.

D-3. Column Entries

a. *Column 1, Group Number.* Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. *Column 2, Component Assembly.* Column 2 contains the noun names of components, assemblies, assemblies, and modules for which maintenance is authorized.

c. Column , Maintenance Function Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumns), the lowest level of maintenance authorized or to perform the function is listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function

vary at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of task-hour specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item, or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance, quality control time in addition *to* the time required to perform the specific task identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C--Operator Crew
O--Organizational
F--Direct Support
H--General Support
D--Depot

e. Column 5 Tools and Equipment. Column 5 specifies by code those common tool sets (not individual tools) and special tools, test, and support equipment needed to perform the designated function.

f. Column 6, Remarks.

D-4. Tool and Test Equipment Requirements (Sec III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate applicable tool *or* test equipment for the maintenance functions.

b. Maintenance Category. The codes in this *co*lumn indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National NATO Stock Number. This column lists the National NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's page number of the tool followed by the Federal Supply Code for manufacturers (-digit) in parenthesis.

D-5. Remarks (Sec IV) (Not applicable)

(Next printed page is D-3)

SECTION II MAINTENANCE ALLOCATION CHART
FOR
GENERATOR, PATTERN - PG-404

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL C	O	F	H	D	(5) TOOLS AND EQUIPMENT	(6) REMARKS
00	GENERATOR, PATTERN PG-404	Inspect	0.2					7	
		Test				0.5		1 thru 6	
		Service	0.4					7	
		Repair	0.2					7	
		Repair				0.5		6	
		Overhaul					3.0	1 thru 6	
01	CHASSIS ASSEMBLY	Test				0.5		1 thru 5	
		Repair				0.4		6	
0101	CIRCUIT CARD ASSEMBLY	Inspect				0.3			
	(TIMING & REGISTER)	Test				0.4		0 thru 1	
		Repair				0 4		6	
0102	CIRCUIT CARD ASSY	Inspect				0.3			
	(DISTORTION & MESSAGE GENERATOR)	Test				0.4		1 thru 5	
		Repair				0.4		6	
02	CASE	Repair				0.5		6	

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS FOR

GENERATOR, PATTERN - PG-404

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	H, D	ANALYZER, DATA, TELEGRAPH TS-3378/G	PENDING	
2	H, D	COUNTER, ELECTRONIC, DIGITAL READOUT AN/USM-459	6625-01-061-8928	
3	H, D	MULTIMETER AN/USM-223	6625-00-999-7465	
4	H, D	OSCILLOSCOPE AN/USM-281C	6625-00-106-9622	
5	H, D	TELETYPEWRITER TT-412/UG	PENDING	
6	H, D	TOOL KIT, ELECTRONIC EQUIPMENT TK-100/G	5180-00-605-0079	
7	C	TOOLS AND TEST EQUIPMENT AVAILABLE TO THE OPERATOR BECAUSE OF HIS/HER ASSIGNED MISSION.		
		*THE NATIONAL STOCK NUMBERS THAT ARE MISSING FROM THIS LIST HAVE BEEN REQUESTED AND WILL BE ADDED BY A CHANGE TO THE LIST UPON RECEIPT.		

APPENDIX E

REPAIR PARTS LIST

Section I. GENERAL

A complete list of replaceable Pattern Generator electronic part is provided below, by major assembly. Within each assembly breakdown, parts are listed in alphanumeric order, by reference designation symbol; for each entry, a brief description and the manufacturer part and code numbers are provided. Manufacturer codes are identified in the following table.

Table 5-1. Manufacturer Codes

Code. No.	Manufacturer
01295	Texas Instruments Inc., Semiconductor and Components Division, Dallas, Texas
26483	Montsanto Co. Inc., West Caldwell, New Jersey
34122	Marathon Battery Co., Coldpring, New York
56289	Sprague Electric Co., North Adams, Massachusetts
70903	Belden Corp., Chicago, Illinois
71400	Bussmann Mfg., Division of McGraw Edison Co., St. Louis, Missouri
75915	Littelfuse, Inc., Des Plaines, Ilinois
80294	Bourns, Inc., Riverside, California
81349	Military Specifications
82389	Switchcraft, Inc., Chicago, Illinois
83330	Herman H. Smith Inc., Brooklyn, New York
86684	RCA Corp. Electronic Component, Harrison, New Jersey
96238	STELMA, Inc., Stamford, Connecticut

Table 5-2. Replaceable Parts

PATTERN GENERATOR ASSEMBLY (97009000-000)

Ref Design	Description	Mfr Code No.	Mfr Part No.
A1	ASSY, CHASSIS:	97009003-000	96238
BT1	BATTERY, STORAGE: 4.8V	38929-10	34122
CR1, CR2	SEMICOND DIODE: silicon;	1N645	81349
F1, F2	FUSE, CARTRIDGE: 1/10 amp;	GMW1-10	75915
F3	FUSE, CARTRIDGE: 1 amp;	312001	75915
R1	RESISTOR, FXD, COMP: 10 ohms, ± 5%, 1W;	RC32GF100J	81349
T1	TRANSFORMER, POWER:	43000290-000	96238
W1	CABLE ASSEMBLY, POWER, ELECTRICAL:	17160S	70903
XF1, XF2	FUSEHOLDER:	HWA-AF	71400
XF3	FUSEHOLDER:	3823-1	71400

CHASSIS ASSEMBLY A1 (97009003-0)

Ref design	Description	Mfr Part No.	Mfr Code No
A1	CKT CARD ASSY, Timing and data register;	87009000-00	96238
A2	CKT CARD ASSY, Distortion and message generator;	87009010-000	96238
C1	CAP., FXD, CERAMIC: 0.25uf, ± 20%, 500V;	5GA-S25	56289
DS1	DIODE: Red Emitting	MV5022	26483
J1	JACK, TELEPHONE:	N111	82389
J2	JACK, BANANA: Red;	1508-102 RED	83330
J3	JACK, BANANA: Black;	1508-103 BLK	83330
Q1	TRANSISTOR: NPN	ST213	96238
R2	RES, FXD, COMP: 1000 ohms, ± 5%, 1/2W;	RC20GF107J	81349

CIRCUIT CARD ASSEMBLY A1A1, TIMING & DATA REGISTER (87009000-000)

Table 5-2. Replaceable Part--Continued

CIRCUIT CARD ASSEMBLY A1A1, TIMING & DATA REGISTER (870090-000)

Ref Design	Description	Mfr Part No.	Mfr Code No.
CR1-CR15	SEMICOND, DIODE: germanium;	1N277	81349
CR16-CR19	SEMICOND, DIODE: silicon;	1N914	81349
C1	CAP, FXD, M1CA: 2000pf, ± 5%, 500V;	CM06FD202J03	56289
C2	CAP., FXD, TANTALUM: 3.3uf, ±20%, 15V;	CS13BD335M	81349
C3	CAP., FXD, CERAMIC: 1000pf, ±20%, 1KV;	C023B102E102M	56289
C4	CAP., FXD, CERAMIC: 0.01uf, ±20 %, 100V;	C023B101F103M	56289
C5	CAP., FXD, TANTALUM: 10uf, ±20%, 20V;	CS13BE106M	81349
C6	Same as C4		
C7	Same as C5		
C8	Same as C2		
C9	CAP., FXD, CERAMIC: 0.005uf, ± 20%, 100V;	C023B101E502M	56289
C10	Same as C2		
Q1-Q3	TRANSISTOR: NPN;	2N2222	81349
Q4	TRANSISTOR: NPN;	2N930	81349
Q5	TRANSISTOR: PNP;	2N2907	81349
R1-R4	RES, VAR: 10, 000 ohms;	3006P-1-103	80294
R5	RES, FXD, FILM: 35.7K ohms, ±1%, 1/10W;	RN55C3572F	81349
R6	RES, FXD, FILM: 301, 000 ohms, ±1%, 1/8W;	RN55D3013F	81349
R7	RES, FXD, COMP: 470 ohm, ± 5%, 1/4W;	RC07GF471J	81349
R8	RES, FXD, COMP: 4700 ohms, ±5%, 1/4W;	RC07GF472J	81349
R9	RES, FXD, COMP: 22, 000 ohms, ±5%, 1/4W;	RC07GF223J	81349
R10	RES, FXD, COMP: 68, 000 ohms, ±5%, 1/4W;	RC07GF683J	81349
R11, R12	RES, FXD, COMP: 39, 000 ohms, ±5%, 1/4W;	RC07GF393J	81349
R13, R14	RES, FXD, COMP: 3900 ohms, ±5%, 1/4W;	RC07GF392J	81349
R15, R16	RES, FXD, COMP: 7500 ohm, ±5%, 1/4W;	RC07GF752J	81349
R17	RES, FXD, COMP: 1K ohms, ±5%, 1/4W;	RC07GF102J	81349
R18	RES, FXD, COMP: 30, 000 ohms, ±5%, 1/4W;	RC07GF303J	81349
R19	RI, FXD, COMP: 5600 ohms, ±5%, 1/4W;	RC07GF562J	81349
R20	Same as R11		
R21, R22	RES, FXD, COMP: 22 ohms, ±5%1/4W;	RC07GF220J	81349
R23-R26	Factory Select (for baud rate)		
S1, S2	SWITCH ASSEMBLY:	46027669-000	96238
T1	TRANSFORMER:	43000289-000	96238
U 1	INTEGRATED CKT: 4-bit binary counter;	SN74L93N	01295
U2	INTEGRATED CKT: cos/mos gates;	CD4001AE	86684
U3-U5	INTEGRATED CKT: 4-bit shift register	SN74L95N	01295
U6	INTEGRATED CKT: hex inverter	SN74L04N	01295
VR1	SEMICOND, DIODE: Zener;	1N756A	81349
VR2, VR3	SEMICOND, DIODE: Zener;	1N759A	81349
VR4	SEMICOND, DIODE: Zener;	1N964B	81349
VR5	Same as VR2		
CR1	SEMICOND, DIODE: silicon;	1N914	81349
CR2	SEMICOND, DIODE: germanium;	1N277	81349
CR3-CR6	SEMICOND, DIODE: silicon;	1N645	81349
C1	CAP., FXD, TANTALUM: 2.2uf, ±20%, 20V;	C13BE225M	81349
Q1	TRANSISTOR: NPN;	2N2222	81349
Q2	TRANSISTOR: PNP;	2N2907	81349
Q3	Same as Q1		
R1	RES, FXD, COMP: 33, 000 ohms, ±5%, 1/4W;	RC07GF333J	81349
R2	RES, FXD, COMP: 15, 000 ohms, ±5%, 1/4W;	RC07GF153J	81349
R3	RES, FXD, COMP: 47, 000 ohms, ±5%, 1/4W;	RC07GF473J	81349
R4	RES, FXD, COMP: 24, 000 ohms, ±5%, 1/4W;	RC07GF243J	81349
R5-R12	RES, FXD, COMP: 22, 000 ohms, ±5%, 1/4W;	RC07GF223J	81349
R13	RES, FXD, COMP: 10, 000 ohms, ±5%, 1/4W;	RC07GF103J	81349
R14	Same as R4		
R15	Same as R13		
R16	Same as R4		
R17	Same as R13		
R18	Same as R4		
R19	Same as R13		

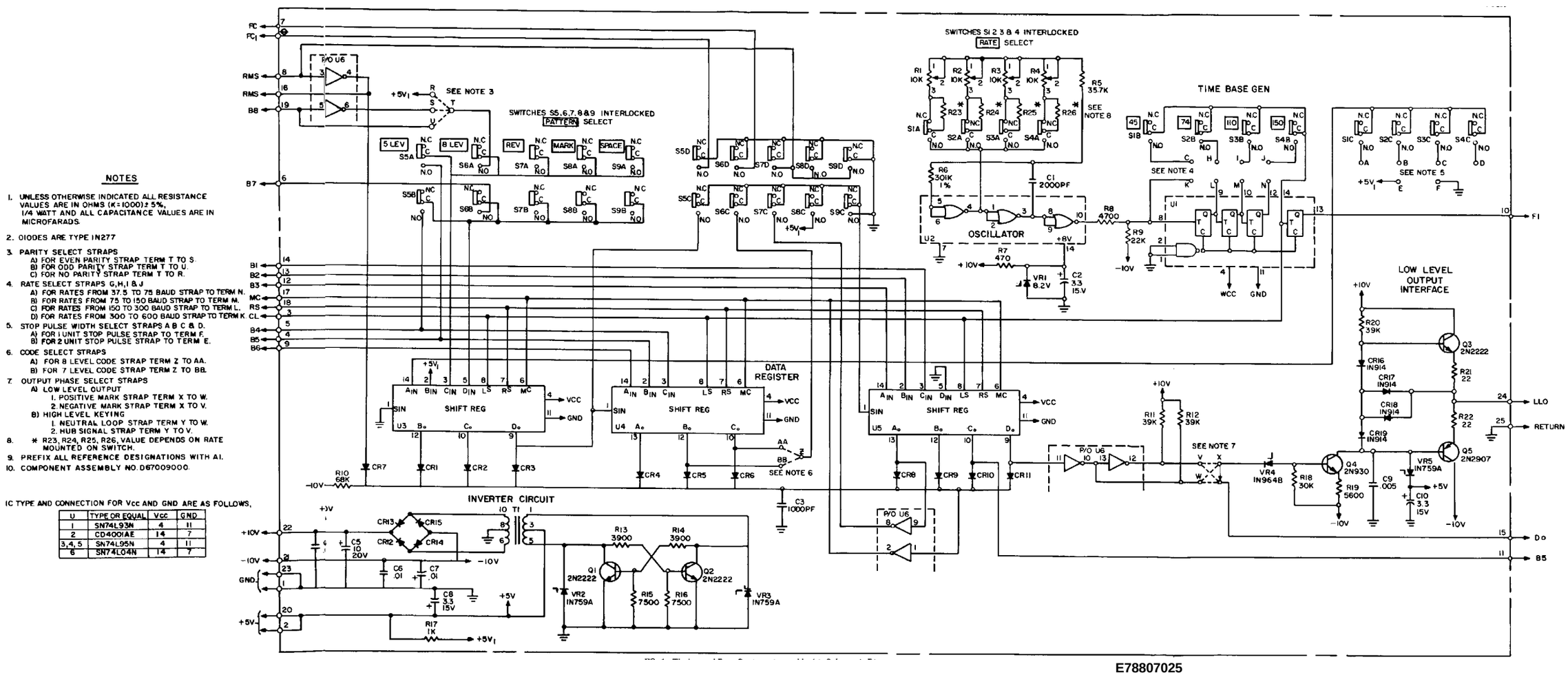
Table 6-2. Replaceable Parts-Continued

CIRCUIT CARD ASSEMBLY A1A1, TIMING & DATA REGISTER, (87009000-000)

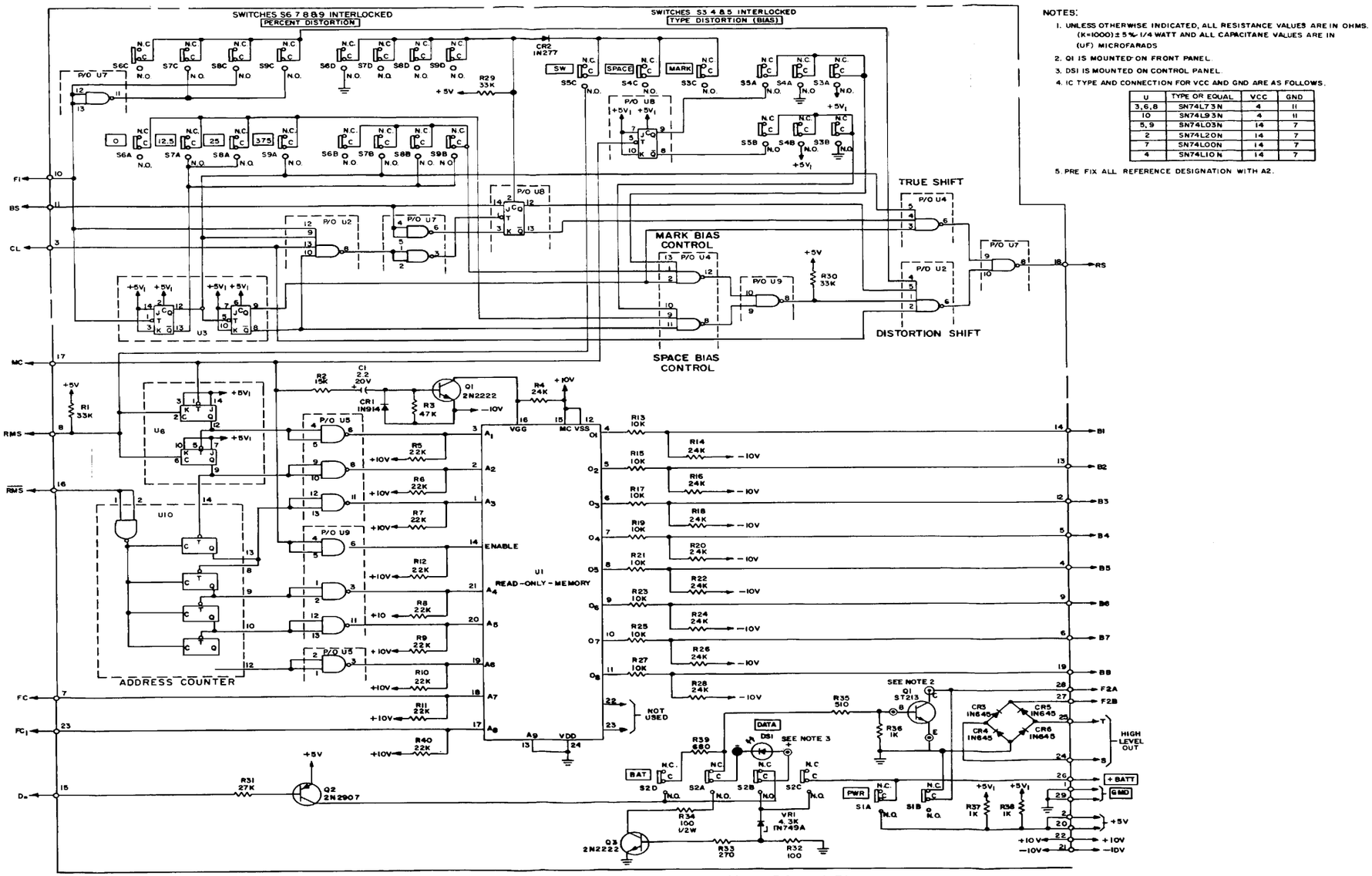
Ref Desig	Description	Mfr Part No.	Mfr Code No.
R20	Same as R4		
R21	Same as R13		
R22	Same as R4		
R23	Same as R13		
R24	Same as R4		
R25	Same as R13		
R26	Same as R4		
R27	Same as R13		
R28	Same as R4		
R29, R30	Same as R1		
R31	RES, FXD, COMP: 27, 000 ohms, ±5%, 1/4W;	RC07GF273J	81349
R32	RES, FXD, COMP: 100 ohms, ±5%, 1/4W,	RC07GF101J	81349
R33	RES, FXD, COMP: 270 ohm, ±5%, 1/4W;	RC07GF271J	81349
R34	RES, FXD, COMP: 100 ohms, ±5%, 1/4W;	RC07GF101J	81349
R35	RES, FXD, COMP: 510 ohm, ±5%, 1/4W;	RC07GF511J	81349
R36-R38	RES, FXD, COMP: 1000 ohms, ±5%, 1/4W;	RC07GF102J	81349
R39	RES, FXD, COMP: 680 ohms, ±5%, 1/4W;	RC07GF681J	81349
S1-S4	SWITCH ASSEMBLY:	46027668-000	96238
U1	INTEGRATED CKT: read-only memory;	45010006-000	96238
U2	INTEGRATED CKT: 4-input NAND gate;	SN74L20N	01295
U3	INTEGRATED CKT: dual J-K master-slave flip-flop;	SN74L73N	01295
U4	INTEGRATED CKT: 3-input NAND gate;	SN74L10N	01295
U5	INTEGRATED CKT: 2-input NAND gate;	SN74L03N	01295
U8	Same as U3		
U7	INTEGRATED CKT: 2-input NAND gate;	SN74L00N	01295
U8	Same as U3		
U9	Same as U5		
U10	INTEGRATED CKT: 4-bit binary counter;	SN74L93N	01295
VR1	SEMICOND, DIODE: Zener;	1N749A	81349

SECTION II. PART NUMBER -- NATIONAL STOCK NUMBER CROSS REFERENCE INDEX

PART NUMBER	FSCM	NATIONAL STOCK NUMBER	PART NUMBER	FSCM	NATIONAL STOCK NUMBER
CD4001AE	86684	5962-00-169-4730	RN55D3013F	81349	5905-00-733-1565
CS13BE106M	81349	5910-00-433-5446	SN74L00N	01295	5962-00-400-9087
CS13BE225M	81349	5910-00-007-2002	SN74L04N	01295	5962-00 497-1586
CS13B101E502M	56289	5910-00-110-7493	SN74L10N	01295	5962-00-169-4723
C023B1F103M	56289	5910-00-810-4849	SN74L73N	01295	5962-00-167-3463
C023B102E102M	56289	5910-00-126-1593	SN74L93N	01295	5962-00-274-4110
N111	82389	5935-00-941-3817	1N645	81349	5961-00-577-6084
RC07GF101J	81349	5905-00-683-7721	1N914	81349	5961-00-022-5664
RC07GF102J	81349	5905-00-681-6462	1N964B	81349	5961-00-752-6115
RC07GF103J	81349	5905-00-683-2238	3006P-1-103	80294	5905-00-243-1778
RC07GF153J	81349	5905-00-681-8818	3823-1	71400	5920-00-137-4991
RC07GF220J	81349	5905-00-755-8389			
RC07GF223J	81349	5905-00-687-0002			
RC07GF243J	81349	5905-00-721-0597			
RC07GF271J	81349	5905-00-725-6995			
RC07GF273J	81349	5905-00-686-3838			
RC07GF303J	81349	5905-00-803-2908			
RC07GF333J	81349	5905-00-686-3903			
RC07GF392J	81349	5905-00-682-4098			
RC07GF393J	81349	5905-00-686-3358			
RC07GF471J	81349	5905-00-120-9154			
RC07GF472J	81349	5905-00-686-9998			
RC07GF473J	81349	5905-00-683-2246			
RC07GF511J	81349	5905-00-116-2394			
RC07GF562J	81349	5905-00-691-0195			
RC07GF681J	81349	5905-00-727-8001			
RC07GF683J	81349	5905-00-681-8853			
RC07GF752J	81349	5905-00-682-4101			
RC07GF102J	81349	5905-00-195-6806			
RC32GF100J	81349	5905-00-279-1692			
RN55C3572F	81349	5905-00-982-0482			



FO-1. Timing and Data Register Assembly A1, Schematic Diagram



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FO-2. Distortion and Message Generator Assembly A2, Schematic Diagram.

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