TM 11-6625-2611-40

TECHNICAL MANUAL

DIRECT AND GENERAL SUPPORT
MAINTENANCE MANUAL
FOR

TEST SET TRANSPONDER SET
AN/APM - 305A
(NSN 6625-01-052-3881)

HEADQUARTERS, DEPARTMENT OF THE ARMY

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GENERAL SUPPORT MAINTENANCE MANUAL

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REPORTING OF ERRORS

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In either case a reply will be furnished direct to you.

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CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope.

a. This manual provides general support maintenance instructions for Test Set, Transponder Set AN/APM–305 (test set). It includes an introduction, a description of the functioning of equipment, general support maintenance instructions, and diagrams. The maintenance instructions cover troubleshooting, removal and replacement instructions, adjustment and alignment procedures, repair instructions, and testing procedures.

b. operational and organizational maintenance instructions are contained in TM 11-6625-2611-12. Repair parts and special tools list are contained in TM 11-6625-2611-24P.

NOTE

For other applicable forms and records see paragraph 1-3 of TM 11–6625–2611–12.

1–2. Indexes of Publications.

a. DA PAM 310-4. Refer to DA PAM 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA PAM 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWOs) pertaining to the equipment.

1–3. Reporting Equipment Improvement Recommendations (EIR).

EIR's will be prepared using SF 368 (Quality Deficiency Report). Instructions for preparing EIRs are provided in TM 38-750, the Army Maintenance Management System. EIR's should be mailed direct to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703. A reply will be furnished direct to you.

Section II. DESCRIPTION AND DATA

1-4. Purpose and Use.

The test set is a bench test set which when used with an Oscilloscope, and Test Set, Transponder Set AN/APM-239, provides field personnel with the capability to check, maintain, align and calibrate the AN/APX-72 Transponder Set and other IFF transponders which meet the requirements of DOD-AIMS 65-1000. The test set generates IFF interrogations and transmits these signals at adjustable RF power levels and adjustable PRF's to the transponder under test. Two separately variable RF outputs are provided to test diversity type transponders, or the two RF paths can be combined to test transponder ISLS characteristics over the complete dynamic range of the transponder. The RF reply from the transponder is demodulated and can be analyzed for proper frequency, power level, coding, pulse shape and pulse train spacing. Mode 4 operation, including disparity conditions, can be simulated. Facilities are also included to test the selectivity of the transponder receiver; test the rate limiting, auxiliary trigger, receiver dead time, and suppression pulse circuits; and supply crystal controlled markers to the oscilloscope. A self test feature permits isolation of failures to a printed circuit card and/or module level using only the test set indicators and test points.

Description of Test Set, Transponder Set AN/APM-305A is covered in TM 11-6625-2611-12 along with unit operation and organizational maintenance. It includes instructions for installation, operation, inspection, self-testing, and preventive maintenance of the equipment.

1-5. Tabulated Data.

Refer to TM 11-6625-2611-12.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. BLOCK DIAGRAM DESCRIPTION

2-1. Overall Function.

The test set facilitates maintenance of IFF transponder sets by generating SIF and MODE 4 challenge signals and detecting the transponder set replies. Replies from the transponder set are then made available by the test set for measurement and. display on an oscilloscope. The test set provides SIF makers which are used to measure pulse spacings of the transponder replies. Timing markers are provided for accurate pulse measurement. Swept rf and markers generated by the test set are used to determine the bandwidth and center frequency of the transponder set receiver and in measuring transponder transmitter frequency. The prf of either the challenge or reply video can be monitored by a meter on the test set. The meter is also used to measure the rf power transmitted by the transponder. Capability is provided for varying all parameters of the challenge signals to evaluate transponder receiver and decoder performance. In addition, separate rf input/outputs are provided for measurement of diversity transponder Characteristic.

2-2. Measuring Modes Fuctional Description.

The test set operates in two basic measurement modes, swept frequency and fixed frequency. Swept frequency is selected by setting the SIG GEN FCTN switch to either SWP ±5 MHZ or SWP ±20 MHZ. In swept frequency, the test set is used to measure transponder receiver bandkvidth characteristics and transponder transmitter frequency. Fixed frequency is selected by setting the SIG GEN FCTN switch to FIXED FREQ and is used to measure all other transponder characteristics.

a. Fixed Frequency. In fixed frequency, the test set interrogates the transponder under test in SIF challenge modes or in mode 4. The transponder SIF or mode 4 reply is detected by the test set and the resultant video is made available for display on an external oscilloscope. In mode 4, in addition to interrogating the transponder and detecting the resultant reply, the test set simulates a mode 4 computer by generating the mode 4 reply in response to a mode 4 enable signal from the transponder. Mode 4 disparity conditions are also simulated. operation of the test set in SIF modes is described in paragraph (1) below. Operation of the test set in mode 4 is described in paragraph (2) below.

(1) *Fixed frequency (SIF) operation (figure 2-1).* In SIF fixed frequency mode of operation, the test set interrogates the transponder in challenge modes 1, 2, 3/A, C and Test. Challenge signals are generated by modulating a 1030 MHz. cw rf with challenge video pulses. The mode of challenge is selected with the test set front panel Controls.

(a) The prf of the test set is established in the prf and delay generator and is selected by the PRF SELECT controls. Outputs from the prf and delay generator trigger the challenge video generation circuits which generate the main and auxiliary modulation video applied to the dual modulator. In addition, the prf and delay generator generates a scope trigger at the MEASUREMENT SCOPE TRIG OUT jack for use by an external oscilloscope. The scope trigger can be delayed by the SCOPE TRIG/FREQ MEAS DELAY (µSEC) controls to facilitate oscilloscope measurement of the reply video.

(b) The 1030 MHz. cw rf is divided within the dual modulator into separate rf outputs which are modulated by the main modulation video (main mod video) and auxiliary modulation video (auxiliary mod video) signals. The modulated rf outputs are applied to the RF IN/OUT MAIN and AUX jacks, through the MAIN ATTEN and AUX ATTEN controls. The auxiliary output is used when testing transponders having diversity capabilities.

(c) For ISLS testing, the rt modulated by the auxiliary mod video signal is combined with the main rf output and both signals are applied to the RF IN/OUT MAIN jack. Under this condition, the MAIN ATTEN controls the level of both signals and the AUX ATTEN controls the level of the ISLS (P2) signal relative to the level of the interrogation pulse pair (P1 and P3).

(d) The SIF reply is received from the transponder through the RF IN/OUT jacks. Inputs to be detected are selected by the DEMOD SEL switch

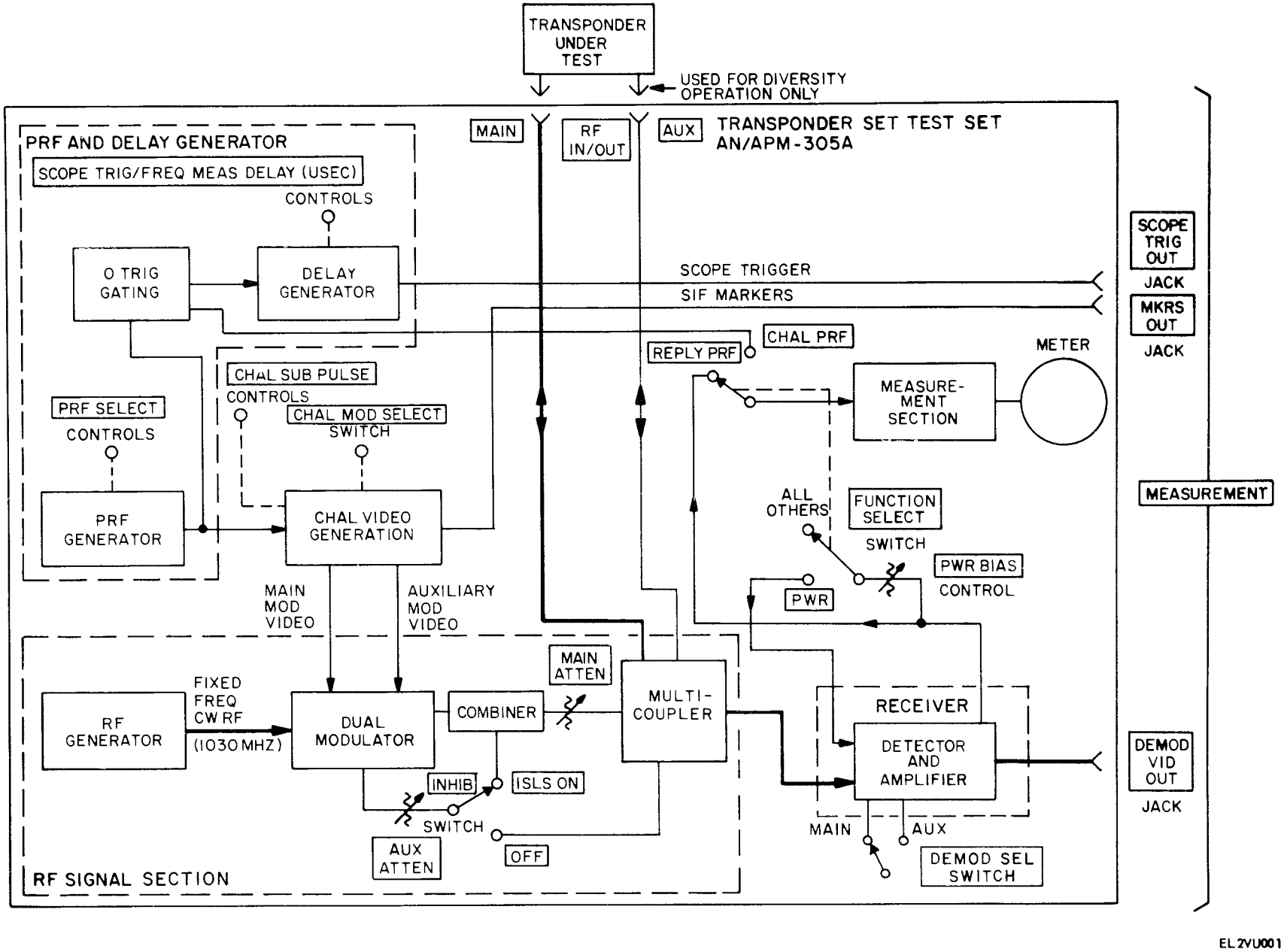


Figure 2–1. Fixed frequency (SIF) operation simplified block diagram

and are detected and amplified. Resultant video is provided at the MEASUREMENT DEMOD WD OUT jack for display on the external oscilloscope. A DC level corresponding to the detected SIF reply is also applied to the measurement section.

(e) When the MEASUREMENT FUNCTION SELECT switch is set to the CHAL PRF, the measurement section translates the challenge prf into a dc voltage which si applied to the MEASUREMENT meter. The dc voltage causes the MEASUREMENT meter to indicate challenge prf in Hz. When the MEASUREMENT FUNCTION SELECT switch is set to PRF REPLY, the MEASUREMENT meter indicates the reply prf. When the MEASUREMENT FUNCTION SELECT switch is set to PWR, the DC level is amplified by a log amplifier and applied to the meter. In practice, the MEASUREMENT DEMOD VIDEO LEVEL control is adjusted until the video at the MEASUREMENT DEMOD VID OUT jack is 1.0 volts in amplitude. The MEASUREMENT meter then indicates peak rf power in dbw.

(f) In fixed frequency operation, the prf generation triggers the challenge video generation circuits to produce challenge video signals. Simultaneously the prf generation gating starts the timing of the delay generator through the 0 trigger gating. The rate at which this cycle occurs is controlled by the PRF SELECT controls. Upon receipt of a start signal the challenge video generation circuit generates a challenge for both the main and auxiliary mode video. The actual challenge mode is controlled by the CHAL MODE SELECT switch. Pulse width is controlled by the CHAL WIDTH ccmtrol. Pulse spacing within each mode is determined by the CHAL SUB PULSE controls. ISLS selected by the INHIBIT switch with its position controlled by the ISLS spacing controls. The auxiliary mode video is delayed from the main mode video by the AUX MOD DLY control to check diversity pulse coincidence characteristics.

(g) Upon completion of the challenge, the challenge video generation circuits provide SIF markers for display on the external oscilloscope. The SIF makers occur at 0, 20.30, 24.65, and 49.30 µsec. The 0 and 20.30 µsec markers are used to measure the spacing of the F1 and F2 pulses of the reply train. The 0 and the 24.65 µsec markers are used to measure the spacing between the F1 and I/P pulse for I/P replies in modes 2 and 3 and between the F1 pulses of the first and second reply trains for mode 1 I/P replies. To meaure reply train parameters during emergency the 0, 24.65 and 49.30 µsec markers are used to measure the spacing between the F1 pulse of the reply and the F1 pulse of the first and second sets of brackets following the reply.

(h) The prf generation which triggered the delay generator causes a delayed output from the delay generator. Delay of the output is controlled by the SCOPE TRIG/FREQ MEAS DELAY (µSEC) controls. A shaped trigger output from the delay generator is applied to the MEASUREMENT SCOPE TRIG OUT jack and used to trigger the sweep of the external oscilloscope. Delay of the oscilloscope sweep is used in observing the characteristics of the reply pulses.

(2) *Fixed frequency (mode 4) operation (figure 2-2).* In mode 4, the test set generates the mode 4 challenge signals in a manner similar to that described previously for fixed frequency (SIF) operation. Upon receipt of a mode 4 challenge, the transponder generates a mode 4 enable signal which is applied to the mode 4 reply generator. If the CHAL INHIB switch is set to OFF, the mode 4 generator generates a three-pulse mode 4 reply delayed 200 µsec. The three-pulse reply is applied to the transponder via the MODE 4 connector to modulate the transponder transmitter. Processing of the transponder reply is similar to that described previously for fixed frequency (SIF) operation. If the CHAL INHIB switch is set to any position except OFF, the mode 4 reply generator is inhibited and the mode 4 disparity generator is enabled. When the CHAL INHIB switch is set to DISPARITY (MOM), the pulse in the 66 µsec position of the challenge word is inhibited and a mode 4 disparity pulse is applied to the transponder coincident with the inhibited pulse. When the CHAL INHIB switch is set to ISLS ON, an ISLS pulse is added to the challenge word and 65 µsec after the mode 4 enable trigger is received the mock 4 disparity generator generates a disparity pulse which is sent to the transponder.

b. Swept RF Operation (figure 2-3). Swept rf operation is used to measure the transponder receiver bandwidth and transmitter frequency. The test set varies the rf frequency of the challenges to check transponder receiver bandwidth. The test set internally compares the transponder reply rf with a sweeping local oscillator to determine reply rf frequency.

(1) *Function Switch Setting.* When the SIG GEN FCTN switch is set to SWP ±5 MHZ (to check transponder reply rf frequency), the rf sweep generator develops a swept rf that sweeps from 1025 to 1035 MHz. When the SIG GEN FCTN switch is set to SWP ±20 MHZ (to check transponder receiver bandwidth) the rf sweeps from 1010 tp 1050 MHz. The rf sweep provides intermediate swept rf to the frequency marker generator which generates the sweep frequency markers (sweep freq markers). The sweep frequency markers correspond to 1010, 1025, 1027, 1029, 1030, 1031, 1033, 1035, and 1050 MHz. Each marker is generated at the time the rf sweep is at the corresponding frequency. At the start of each sweep, the rf sweep is generated from a sweep sync clock

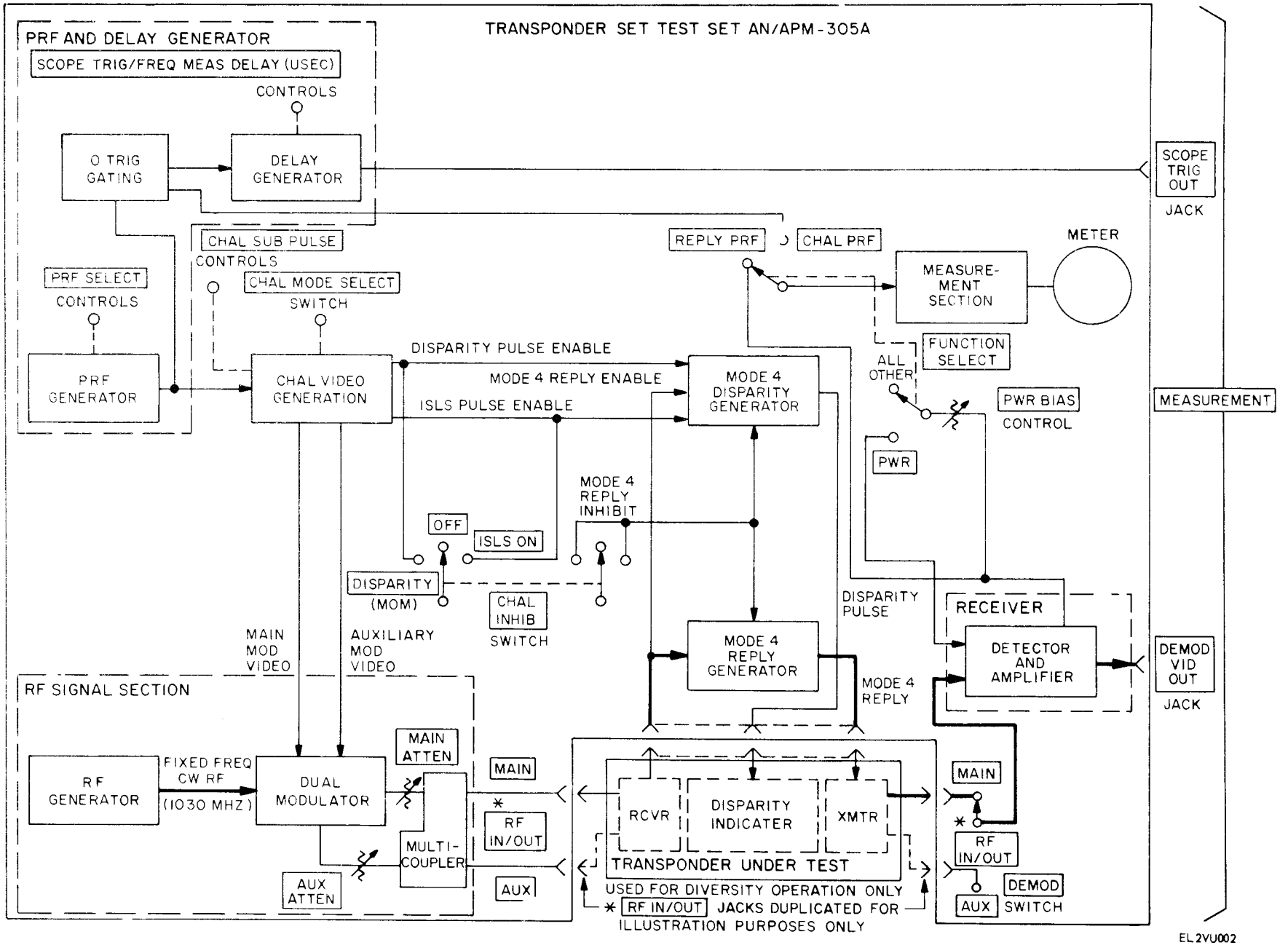


Figure 2–2. Fixed frequency (Mode 4) operation simplified block diagram

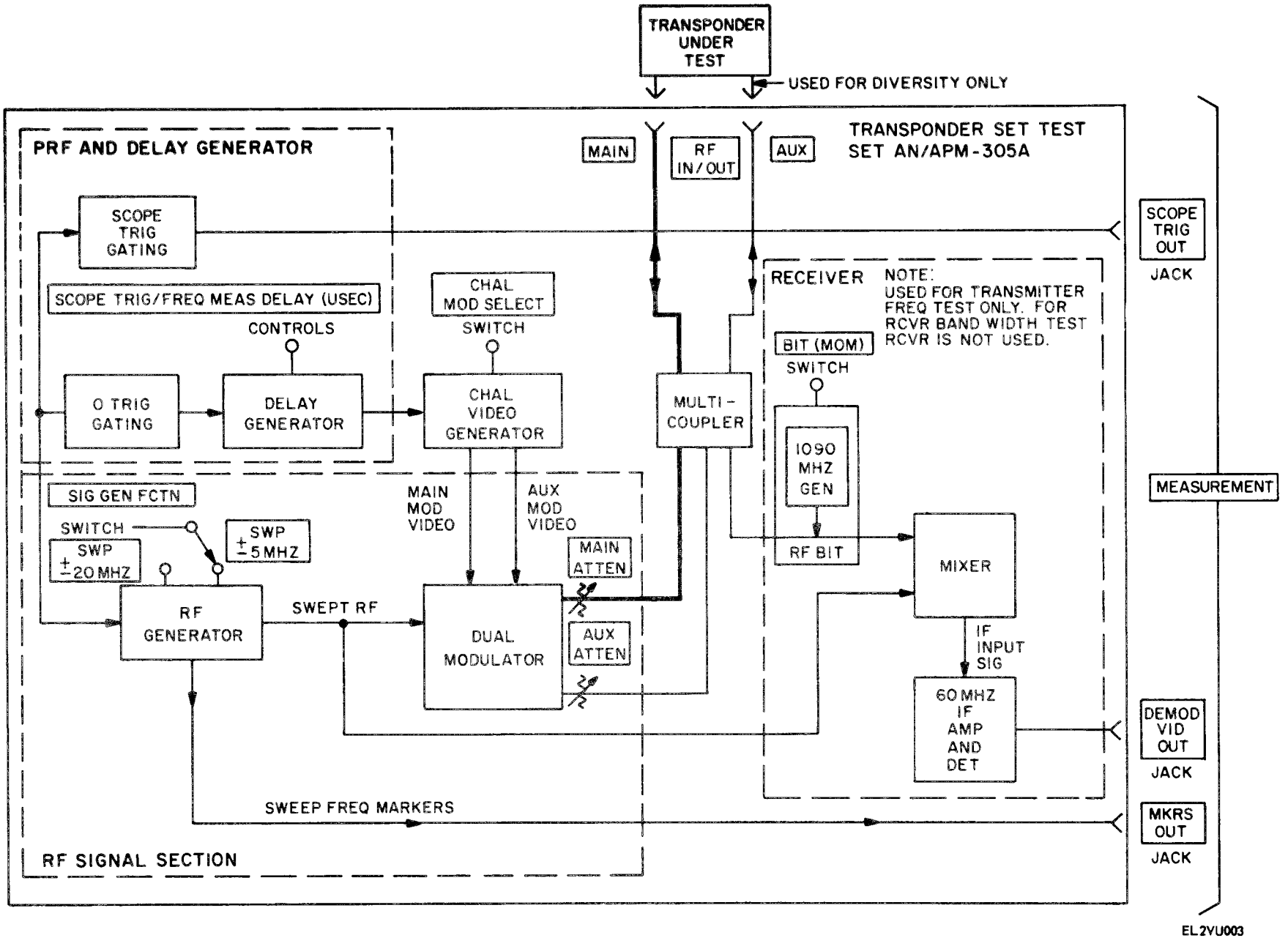


Figure 2–3. Swept frequency operation simplified block diagram

signal generated in the PRF and delay generator.

(a) The swept rf is divided within the dual modulator to provide two separate rf outputs which are modulated by the main and auxiliary mod video signals from the challenge video generator. Modulated rf outputs are applied to the RF IN/OUT MAIN and AUX jacks through the MAIN and AUX ATTEN controls.

(b) The delay between sweep sync signal and the challenge video generation is used to control the rf frequency of the challenge. The delay is adjusted by the SCOPE TRIG/FREQ MEAS DELAY (μSEC) controls. The longer the delay, the higher the rf frequency of the challenge. As the challenge is delayed from the start of sweep, the transponder reply is also delayed. Thus, the frequency difference between the transponder reply rf (which is fixed in frequency) and the swept rf (from the rf sweep generator) is also controlled by the delay. When this difference frequency is 60 MHz a video signal is passed to the DEMOD VIDEO OUT for display on the associated oscilloscope.

(c) The sweep sync signal triggers the oscilloscope through the scope trigger gating and the MEASUREMENT SCOPE TRIG OUT jack.

(2) *Transmitter frequency testing (figure 2–4).* When measuring transponder transmitter rf frequency, the reply from the transponder is applied to the input of the test set receiver through the RF IN/OUT MAIN and AUX jacks and the input to be observed is selected by the DEMOD select switch. The reply rf is mixed with the swept rf by the mixer to form the i-f input signal. The i-f input signal is applied to the 60 MHz i-f amplifier and detector. Because the 60 MHz i-f amplifier has a narrow bandwidth, only 60 MHz signals are amplified. Delay of the challenge and corresponding transponder reply are adjusted using the SCOPE TRIG/FREQ MEAS DELAY (μSEC) controls until the reply signal is 60 MHz from the instantaneous value of the swept rf. This is accomplished by adjusting the SCOPE TRIG/FREQ MEAS DELAY (μSEC) controls until the detected reply video peaks. The position of the reply is then compared with the sweep frequency markers as shown in figure 2–4 to determine the reply rf frequency. Because the reply rf is displaced 60 MHz from the swept rf, the markers correspond to 1085, 1087, 1089, 1090, 1091, 1093, and 1095 MHz for transmitter frequency measurement. The rf frequency of the reply SIF shown in figure 2–4 is 1090 MHz since the detected reply video peaked at a point coincident with the 1090 MHz marker. If the peaked reply video were not coincident with one of the markers, the frequency could be determined by interpolation.

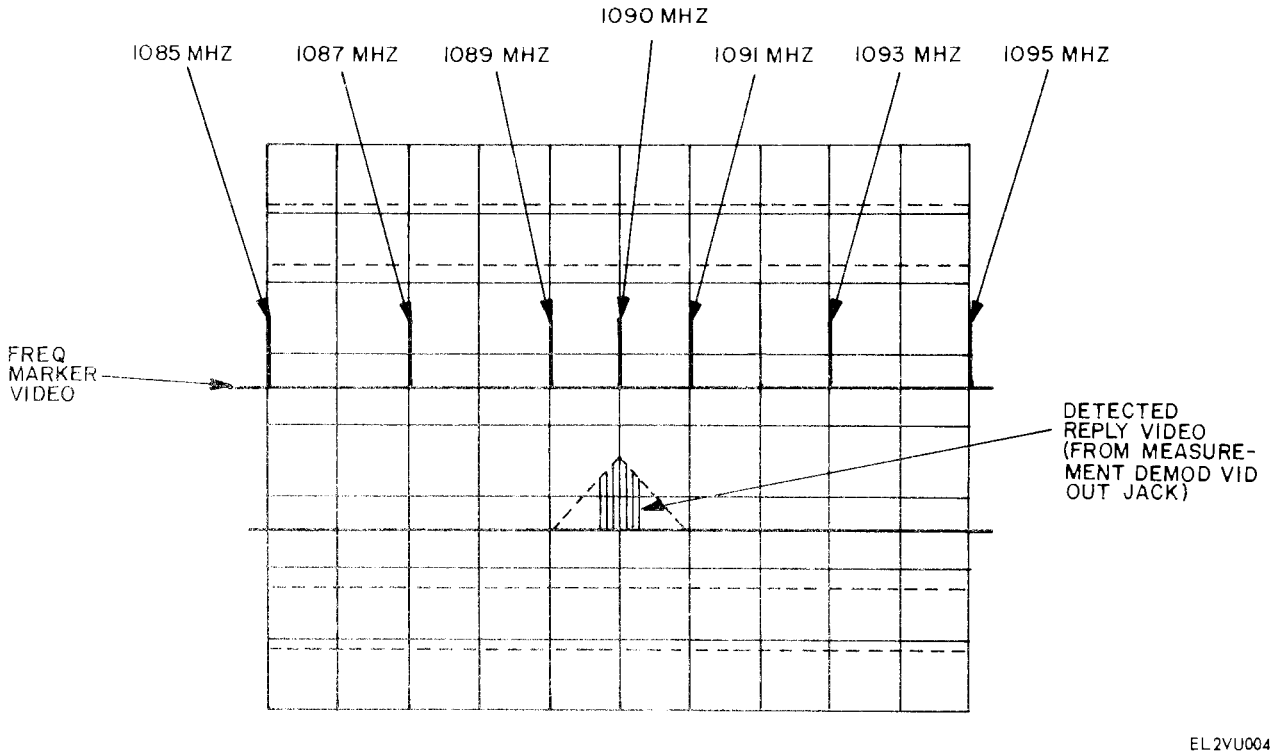


Figure 2–4. Transmitter frequency measurement oscilloscope display

(3) *Transponder bandwidth and center frequency testing (figure* 2-5). Two methods are available for measuring the bandwidth and center frequency of a transponder. One measures the overall bandwidth of the transponder equipment, including its decoder, and can be measured without internal connections to the transponder. The second method measures the bandwidth of the transponder receiver only and is used for receiver alignment. This second method requires a connection between the transponder detector test point and the oscilloscope. For both methods the delay of the challenge is adjusted, using the SCOPE TRIG/FREQ MEAS DELAY (µSEC) controls to vary the frequency of the challenges. For the overall bandwidth measurement, the MAIN ATTENUATOR *is* set to *6* dB above minimum transponder sensitivity and the MEASUREMENT FUNCTION switch is set to PRF REPLY. The SCOPE TRIG/FREQ MEAS DELAY (µSEC) is varied to locate the two frequencies at which the transponder replies to 90% of the challenges as observed on the MEASUREMENT meter. For the transponder receiver only measurement the CHAL MODE SELECT switch should be set to CW and the response curve is set so that the peak signal is aligned with graticule line on the oscilloscope. Then the MAIN ATTEN is decreased by 6 dB and the two frequencies measured by locating the frequency where the response curve crosses the reference graticule line on the oscilloscope.

c. Self Test. By jumpering from the RF IN/OUT

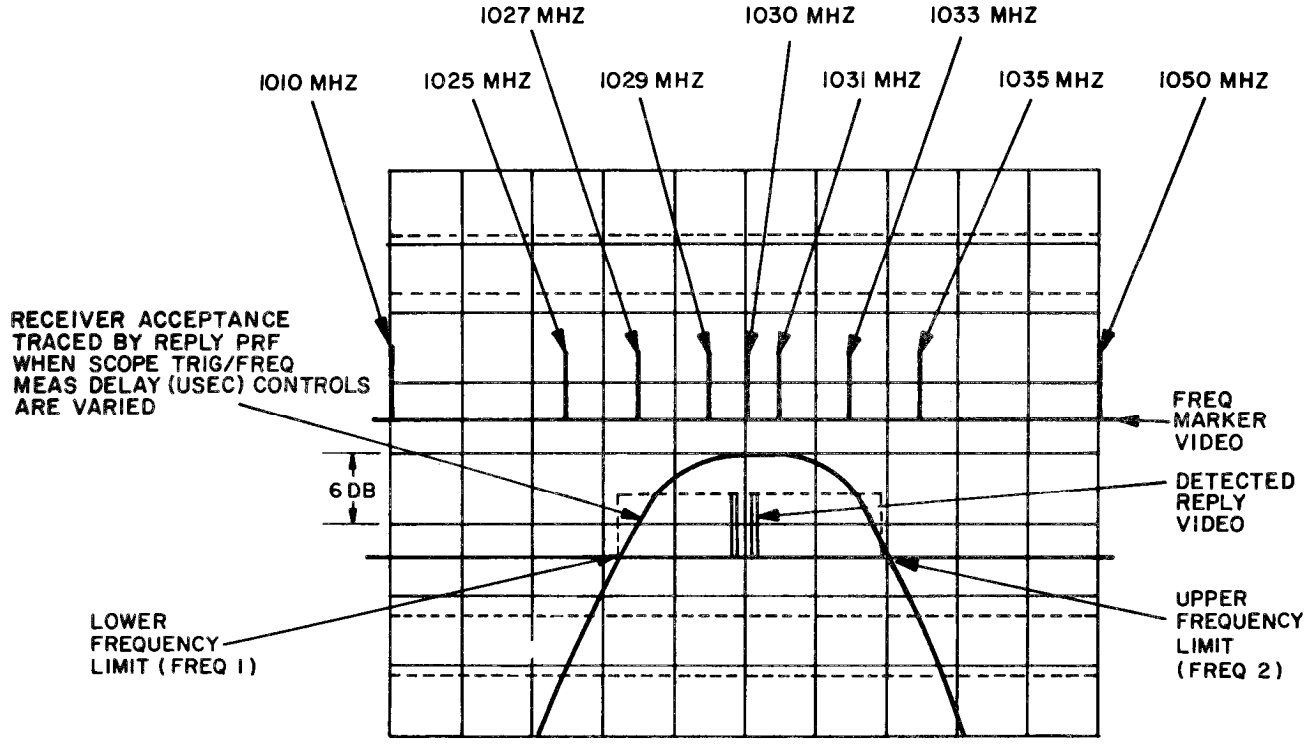


Figure 2–5. Receiver bandwidth testing oscilloscope display

MAIN or AUX jacks to the LOW PWR IN jack the test set will receive its own signals for display on an oscilloscope. This permits testing of all circuitry within the test set except for the frequency measurement circuitry (i. e., mixer, 60 MHz i-f amplifier and associated video detector). This circuitry is tested by activating the BIT (MOM) switch which applies a 1090 MHz signal to the mixer. The BIT (MOM) switch is also used to trigger the mode 4 reply circuitry instead of the mode 4 enable trigger normally received from the transponder.

2-3. Block Diagram.

(FO-2)

Tine test set is composed of six basic sections, the prf and delay generator, the video generator, the rf signal generator, the receiver, the measurement section, and the power supply. A test set cable connection diagram is shown in figure 2-6.

a. Prf and Delay Generator. The prf and delay generator establishes the basic prf at witch the test set operates and generates timing signals used throughout the test set. Gated clock and counter initialize signals are generated and applied to the video generator. The gated clock signals developed by a 1-MHz crystal-controlled clock are applied to the video generator counters to determine timing of the video signals. The counter initialize signals reset the video generator counters. Settings of the PRF SELECT RANGE and MULT controls drtermirre the rate of the counter initialize signals. Also generated are the scope trigger which is provided at the MEASUREMENT SCOPE TRIG OUT jack, the suppressor pulse at the SUPPR OUT jack, and the auxiliary trigger at the AUX TRIG OUT jack. A delay circuit delays initiation of video signals with respect to the scope trigger so that the complete reply video signal can be displayed on expanded scales of the oscilloscope. The amount of delay is controlled by the SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE and MULT controls. Setting the test set to swept frequency operation inhibits the trigger circuits of the prf and delay generator outputs. During swept frequency (operation, the delay is used to control the initiation of the challenge signal.

b. Video Generator.

(1) The video generator provides coded video signals in response to counter initialize and gated clock signals from the prf and delay generator. The gated clock signals determine the time intervals between pulse, and are used to step 7-and 11-bit shift register counters. Outputs of the counters are decoded into the proper pulse intervals. Pulse width at the video signals is determined by the settings of the CHAL, WIDTH SELECT and VARY controls. The CHAL SUB PULSE SELECT and POSITION SELECT and VARY controls vary the positioning of the first pulse of the SIF challenge video or the second, third, or fourth pulse of the mode 4 challenge pulse train. Varying the position of these pulses determines the limits at which the transponder under test will accept a challenge signal. Mode 4 challenge and reply video are provided to test the mode 4 circuits of the transponder. All challenge mode video is applied to the rf signal generator as main and auxiliary mode video. When the CHAL INHIB switch is set to ISLS ON, the auxiliary mode video output is inhibited and the ISLS pulse is substituted. The main and auxiliary rf outputs are combined as the main challenge rf signal.

(2) In fixed frequency operation, the video generator also provides SIF markers at the MKRS OUT jack. These start at a nominal 3 µsec after the completion of the challenge video signal and are controlled by the MEASUREMENT MKR PHASING control. The markers are spaced at 0, 20.3, 24.65, and 49.3 µsec. When the test set is set to swept frequency operation, the SIF markers are inhibited by a marker inhibit signal from the rf signal generator and the sweep freuueney markers are substituted.

c. RF Signal Generator.

(1) The rf signal generator generates fixed frequency rf at 1030 MHz, or swept frequency rf varying from 1025 to 1035 MHz or 1010 to 1050 MHz. The rf is modulated by video from the video generator except when the CHAL MODE SELECT switch is set to CW. It also provides a local oscillator signal to the receiver section which is mixed with the incoming reply rf used to determine reply rf frequency when the MEASUREMENT FUNCTION SELECT switch is in the FREQ position.

(2) During swept frequency operation, the rf signal generator provides an inhibit signal to the video generator to inhibit the SIF reply outputs between sweep times. A sweep sync clock is generated by the PRF and delay generator and is applied at the beginning of each rf sweep to sync the RF sweep and the various video outputs. The rf signal generator also generates sweep frequency markers which occur at 1010, 1025, 1027, 1029, 1030, 1031, 1033, 1035 and 1050 MHz for SWP ±20 MHZ. For SWP ±5 MHZ the 1010 and 1050 MHz markers are not generated.

(3) In swept or fixed frequency operation, the video generator main and auxiliary mod Video modulates the corresponding rf output. The main and auxiliary rf outputs provide for testing of transponders with diversity capability. To determine the ability of a diversity transponder receiver to select the correct reply antenna when the two interrogations are not received simultaneously, the time position of the modulation on the auxiliary output can be varied by the CHAL AUX MOD DLY control.

(4) When the CHAL INHIB switch is set to ISLS

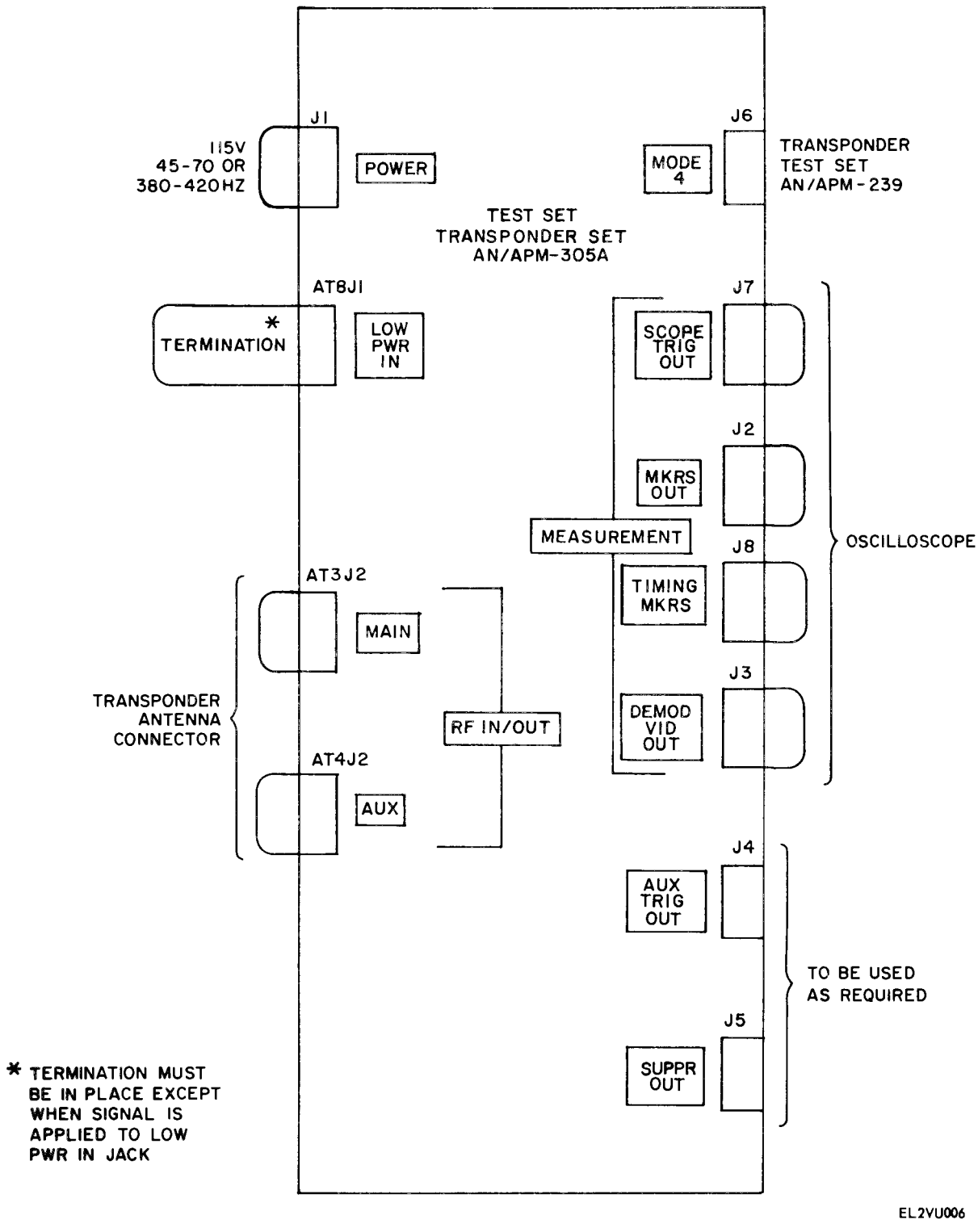


Figure 2-6. Test set cable connection diagram

ON, the ISLS pulse modulates the auxiliary rf section and the auxiliary rf is combined with the main rf output. The AUX ATTEN control sets the relative amplitude of the ISLS pulse and the MAIN ASTTEN control setting determines the overall level of the output rf.

(5) Pressing the BIT (MOM) switch is swept frequency operation, activates an internal self-test rf generator, whose output is mixed with the local oscillator signal. The resultant signal provides a self-test of portions of the rf signal generator, receiver, and measurement sections.

d. Receiver. The receiver accepts rf from the LO PWR IN jack, RF IN/OUT MAIN and AUX jacks. The RF IN/OUT DEMOD switch inhibits or enables signals from either the RF IN/OUT MAIN or AUX jacks. The rf is detected, and the resultant video applied to the MEASUREMENT DEMOD VID OUT jack. The reply prf signal is applied directly to the measurement section for prf display.

e. Measurement *Section.* The measurement section accepts reply prf and power bias signals from the receiver and challenge prf from the prf and delay generator. The input to be measured is selected with the MEASUREMENT FUNCTION SELECT switch. The output of the measurement section is applied to the MEASUREMENT meter for display. For prf measurements, the meter scale factor is set by the MEASUREMENT PRF RANGE switch. For power checks the detector reverse-bias is adjusted by the MEASUREMENT DEMOD VID LEVEL control until the output video is 1.0 volt in amplitude. The level is read out on the MEASUREMENT meter as an indication of the reply signal power level.

f. Power Supply. The power supply receives primary power (115v, 60 or 400 Hz) through the POWER connector and develops the dc voltages necessary to operate the test set. Power is appfied through the POWER ON/OFF switch. The power supply input is fused to provide circuit overload protection and a neon lamp in the fuse holder lights if the fuse opens. Should any of the power supply outputs malfunction, the POWER DC FAULT indicator lights to indicate the malfunction. Each power supply output is current limited to provide for circuit overload protection. The POWER DC FAULT indicator has a press-to-test feature to test the operation of the indicator.

Section II. FUNCTIONAL DESCRIPTION

2-4. Prf and Delay Generator.

a. General.

(1) The prf and delay generator operates in either fixed frequency or swept frequency mode.

(2) In SIF fixed frequency mode, SIF challenge words are generated at a prf established by the signals from prf generator Al. In mode 4 fixed frequency mode, challenge words are generated at the prf established by the prf generator Al. The prf and delay generator also generates the suppressor pulse at the beginning of each challenge word. The delay trigger, A2, delays the generation of the scope trigger at the SCOPE TRIG OUT jack so that the output of the transponder being tested can be observed. The signal at the AUX TRIG OUT jack is generated by the prf and delay generator, and occurs 4 µscc after the prf generator signal initiates the start of a challenge) word cycle.

(3) With the SIG GEN FCTN switch set to either SWP ± 5 MHZ or SWP ±2O MHZ, the sweep generator and timing markers (A9)) generate a sweep signal which is applied to the clock and trigger A3. The scope trigger and suppressor pulse are generated upon receipt of the sweep syne clock signal. Generation of the challenge word is then determined by the delayed trigger.

b. Fixed Frequency Operation (FO-3)

(1) *Prf generator A1.* Prf multivibrator Q14/Q15, prf range gates Q3/Q4, Q5/Q6, Q7/Q8, and PRF SELECT RANGE switch S5 establish the prf range limits. Selection is done using PRF SELECT RANGE switch S5. Three ranges are available, 10 to 110 Hz, 100 to 1100 Hz, and 1000 to 11,000 Hz. Q3/Q4, Q5/Q6, and Q7/Q8, when enables by the PRF SELECT RANGE switch, provide a current source and select the prf multivibrator capacitors, thereby determining the multivibrator charging rate. PRF SELECT MULT control R3 provides a continuous prf adjustment within the selected range. PRF SELECT MULT control R3 applies a regulated voltage to emitter follower Q1/Q2. The emitter follower output is a reference voltage and is applied through gates Q1l/Q12 to prf multivibrator Q14/Q15. This reference voltage establishes the charging voltage of the multivibrator. The upper limit of the reference voltage is set by potentiometer R3. The output of OR gate Q9/Q10/Q13 triggers Q14/Q15 at the prf rate and ensures self-starting of the multivibrator. Potentiometers R19, R14, and R9 adjust the multivibrator time constant for the 10 to 110 Hz, 100 to 110 Hz, and 1000 to 11,000 Hz ranges respectively.

(2) Clock and trigger logic A3.

(a) SIF operation. The following description applies to all SIF modes except dual 3/A. Refer to figure 2-7 for waveform timing diagram.

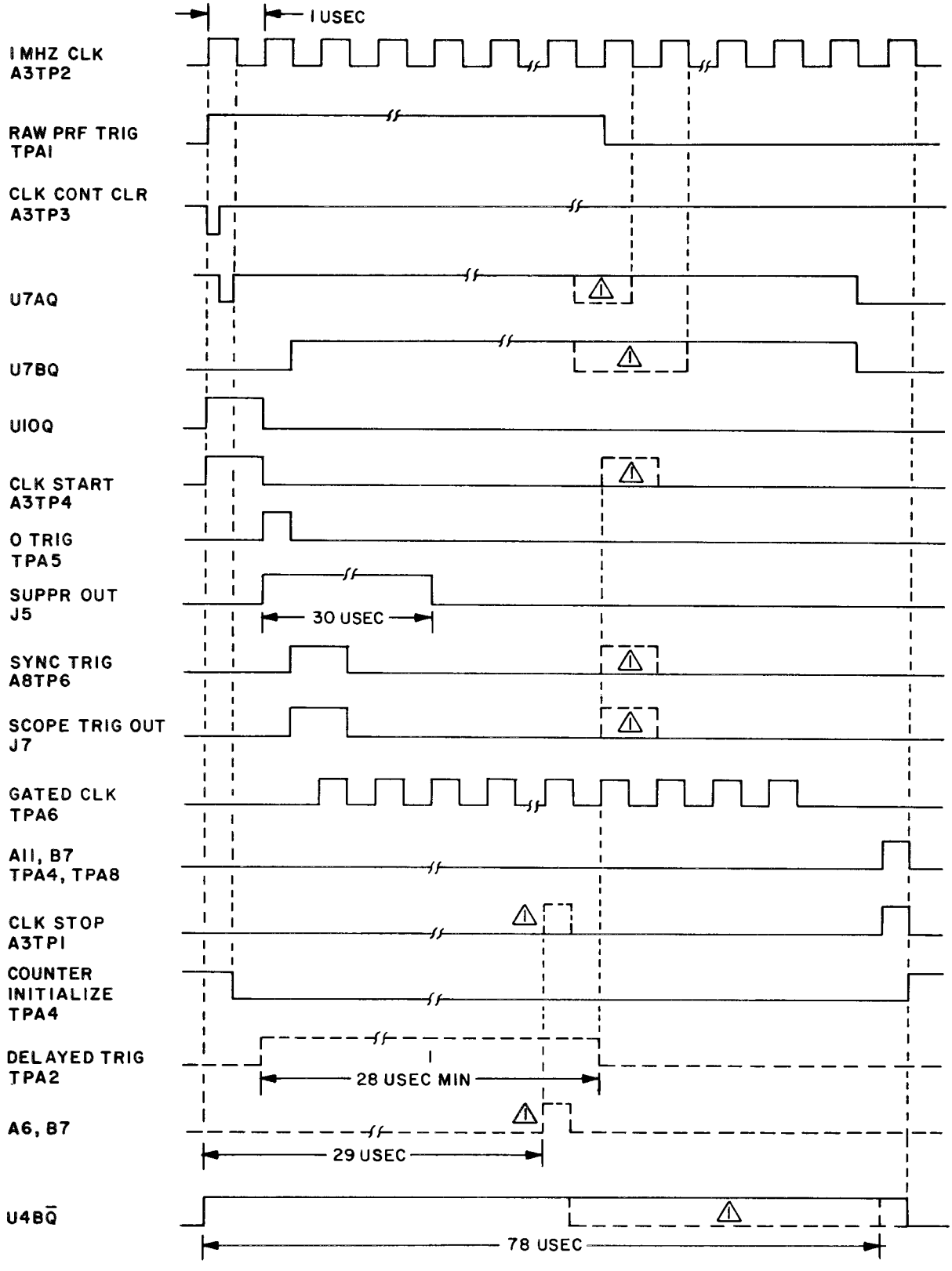


Figure 2-7 SIF fixed frequency clock and trigger logic timing diagram

1 Upon receipt of the raw prf trigger, buffer amplifier Q1 triggers trailing edge generator U12B/U1B, generating the clock control clear signal which clears clock control flip-flops U7A and U7B, and dual mode 3/A flip-flop U4B. The clock control clear signal also triggers raw prf one-shot U10. For all positions of CHAL MODE SELECT switch S3, the raw prf one-shot output is gated through U11A, U11B, U11C, and U2A, to start generation of gated clock pulses.

2 On the fall of the 1 MHz clock generated by Y1/Q1/U3/U4A of A9, the clock start signal sets flip-flop U7A, and the counter initialize signal goes low, enabling the video generator counters.

3 On the rise of the next 1 MHz clock, the output of gate U6A goes low; the () trigger goes high and is applied to one-shot U9/U5D, gate U13B, and delay trigger A2. With SUPPR switch S13 set to ON, the one-shot is triggered, generating the suppressor pulse at the SUPPR OUT jack. With SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch S6 set to OFF, the undelayed 0 trigger signal is gated through U13B and U13C, triggering one-shot U15A on the fall of the clock and triggering U16 generating the scope trigger at the MEASUREMENT SCOPE TRIG OUT jack. Also on the fall of the clock, flip-flop U7B is set and the next clock applied to gate U5C generates a gated clock pulse to the video generator. Subsequent clock pulses to U5C generate additional gated clock pulses for generation of challenge words.

4 The pulses are generated until the clock control flip-flops receive a stop signal from the video generator. When this occurs, A11 and B7 go high, raising clock stop, and flip-flops U7A and U7B reset on the next clock, inhibiting gate U5C. The counter initialize signal goes high, presetting the video generator counters. The SIF operation described is repeated for each raw prf trigger input.

(b.) Mode 4 operation. With PRF SELECT switch S23 set to X1/2, gate U11A is inhibited and gate U12A enabled. On receipt of the raw prf trigger, the trailing edge of the buffer amplifier output clocks and sets mode 4 prf ÷ 2 flip-flop U4A. The raw prf one-shot U10 output is now gated through U12A, U11B, U11C, and U12A and 0 trigger, suppressor pulse, scope trigger, and gated clock pulse's are generated as previously described, Since flip-flop U4A toggles on each raw prf trigger input, the selected prf rate is halved, as only every other pulse of one-shot U10 generates a clock start pulse to the clock control flip-flops. The clock stop pulse comes through as previously described.

(c) Dual mode 3/A operation. (See figure 2-7 for waveform timing diagram). With CHAL MODE SELECT switch set to DUAL 3/A, gates U2B and U13D are enabled and the test set generates two mode 3/A challenge words for each raw prf trigger input. The spacing between each challenge word is determined by the settings of the SCOPE TRIG/FREQ MEAS DELAY (µSEC) controls.

1 In dual mode 3/A operation, the delay controls are set for a delay greater than 30 µsec. Setting the controls inhibits gate U13B and enables gate U13A. The output of the prf generator still initiates gated clock operation and the 0 trigger triggers one shot A2Q9 through Q12.

2 When video generator outputs B7 and A6 go high, a clock stop pulse is generated on the next clock, and flip-flops U7A and U7B reset and flip-flop U4B sets inhibiting gate U6A. The resultant delayed trigger from A2 is gated through U13A and triggers one-shot U15A, generating a scope trigger pulse. The sync trigger is gated through U13D, raising clock start and enabling the generation of the second mode 3/A challenge word.

(d) Auxillary trigger output operation. In all modes of fixed frequency operation, setting AUX TRIG switch S14 to ON enables gate U6B. Four µsec after the start of each challenge word, video generator outputs A4 and B4 go high, generating the auxiliary trigger.

(3) Delay trigger A2. Delay trigger A2 establishes and controls the delay between the challenge word and the scope trigger.

1 Upon receipt of a 0 trigger, the delay time interval selected by the SCOPE TRIG/FREQ MEAS DELAY (µSEC) controls is initiated and at the end of that time, a delayed trigger is generated.

2 The interval timing is performed by one-shot Q9 through Q12. The period of the one-shot is determined by selecting a constant current source with SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch S6. SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control R4 varies the bias of the constant current sources. The timing interval for the step ranges can be varied by simultaneous varying the one-shot supply voltage and the bias level applied to the constant current sources.

3 As previously described, when the SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch is set to OFF, the inhibit in delay signal enables gate A3U13B, and the () trigger is gated directly to the MEASUREMENT SCOPE TRIG OUT jack. Setting the SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch to any other position inhibits gate A3U13B, enables gate A3U13A and selects one of the constant currrent sources (Q5 through Q8). The current available from each source is controlled by reference voltage bias source Q1 through Q4 which is also the variable supply voltage for one-shot Q9 through Q12. The 0 trigger triggers the one-shot and the output of delay output amplifier Q13 goes high. (delayed trigger). The delayed trigger is gated through A3U13A and A3U13C to one-shot A3U15A.

At the end of the selected delay interval, the delayed trigger drops, triggering one-shot A3U15A which generates a scope trigger.

c. Swept Frequency Operation (FO-4)

(1) Setting SIG GEN FCTN switch S17 to either SWP ± 5 MHZ or SWP ± 20 MHZ switches the clock and trigger logic A3 to swept frequency operation. The fixed enable signal goes low inhibiting gate U11C which effectively inhibits the raw prf triggers from prf generator A1. The sweep enable signal generated by U5A goes high enabling the prf and delay generator sweep frequency logic.

(2) The sweep generator and timing marker sweep sync clock signal triggers one-shot U15B which generates a pulse at the MEASUREMENT SCOPE TRIG OUT jack, the SUPPR OUT jack (if SUPPR switch is ON) and triggers delay trigger A2. The operation of delay trigger A2 is described in paragraph 2-4b. The delay trigger output triggers one-shot U15A through gate U13A when delay is enabled. If the delay is inhibited, one-shot U15A is triggered by the 0 trigger through gate U13B. The one-shot output generates the clock start signal, and when the AUX TRIG switch is ON, a pulse at the AUX TRIG OUT jack. The clock control operation is described in paragraph 2-4b.

2-5. Video Generator (FO-5)

In response to the counter initialize and gated clock signals, the video generator develops challenge word signals, SIF marker signals and mode 4 interface signals. The challenge word signals are used to modulate the main and auxiliary rf outputs of the rf signal generator. The SIF markers are used in fixed frequency operation to measure the reply spacing parameters of the transponder under test. The mode 4 interface simulates a mode 4 computer acceptance signal by generating a 3-pulse reply in response to the mode 4 enable trigger from the transponder under test. The mode 4 interface also generates disparity signals used in testing transponders.

a. Challenge Word Generation.

(1) *Fixed pulse position operation.*

(a) The challenge word is selected using CHAL MODE SELECT switch S3. Upon receipt of the counter initialize signal from the prf and delay generator the A- and B- counters (sheet 1) are enabled, terms A1 and B1 go high. The gated clock pulses are at one-µsec intervals, and upon receipt of each clink pulse, the bit set initially into each shift register is clocked into the next position. The first clock pulse which occurs after the counters are enabled, causes terms A1 and B1 to go low and causes terms A2 and B2 to go high. The next clock pulse causes terms A2 and B2 to go low and causes terms A3 and B3 to go high. This action continues until both terms All and B7 are high (occurs ast 76th clock pulse) at which time a clock stop signal is generated within the prf and delay generator. The clock stop signal inhibits any further gated clock pulses from the prf and delay generator. The generation of counter terms in this manner ensures that only one All and B7 counter output is coincident for any one gated clock time. This is easily seen using FO-6, i.e., at the fourth clock pulse, only terms A5 and B5 are high; at the 19th clock pulse only terms A8 and B5 are high; and the 31st clock pulse, only terms A10 and B4 are high. Thus, as can be seen from FO-6, the following signals are generated, based upon the A- and B- counter outputs:

Auxiliary trigger signal.
SIF challenge fixed pulses.
SIF substitute pulse triggers.
SIF marker triggers.
Mode 4 word A and word B pulses.
Mode 4 substitute pulse triggers.

(b) With CHAL MODE SELECT switch S3 set to 1, gate A5U13A is enabled and generates the P1 pulse. The inhibit in A/B signal from CHAL MODE SELECT switch S3 enables gate A5U16B which generates the P3 pulse. When A- and B- counter outputs A2 and B3 are high, P1 is generated by gate A5U13A. When counter outputs A5 and B6 are high, P3 is generated by gate A5U16B. The P1 and P3 pulses for modes 2, 3/A, and C are generated in a similar manner. The P1 pulse for the test mode of operation is generated by gate A6U8 (Sheet 3), delayed by one-shot A6U10, and applied through gate A6U5D to gate A7U2B. The test mode P3 pulse is generated as described for the other SIF modes. The P1 and P3 pulse spacing for the generated challenge word is nominally as follows:

Mode 1:	3.0 µsec
Mode 2:	5.0 µsec
Mode 3/A:	8.0 µsec
Mode C:	21.0 µsec
Test Mode:	6.5 µsec

(c) The mode 4 (A or B) challenge word consists of a series of pulses (28 total) spaced as indicated in FO-6. Pulses or terms which are common to both 4A and 4B are enabled through gate A5U9C (FO-5, Sheet 1) by the inhibit in SIF signal from the CHAL MODE SELECT switch S3. Pulses or terms which are unique to mode 4A are enabled through gate A5U9A when the CHAL MODE SELECT switch is set to 4A. Unique terms of mode 4B are enabled through gate A5U9C when the CHAL MODE SELECT switch is set to 4B.

(d) The P1 and P3, or mode 4 pulses, are applied to gate A5U10B and generate the challenge

word A/B gate (chal word A/B gate) signal. The chal word A/B gate signal is combined with the gated clock signal by gate A7U1A (FO-5, Sheet 2) and applied through gate A7U2B to main offset one-shot A7U6 and auxiliary delay one-shot A7U3.

(e) Main offset one-shot A71J6 delays the main modulation and then trigger-s main shaper one-shot A7U7. The delay places the main modulation within the range of the auxiliary modulation. The output pulse width of one-shot A7U7 is determined by CHAL WIDTH SELECT switch S4. The output, of A7U7 is gated through A7U1B, and modulates the rf signal generator main rf output.

(f) The duration of the auxiliary delay one-shot A7U3 output is determined by CHAL AUX MOD DLY control R8. Varying the output duration of A7U3 varies the position of the auxiliary modultion in relation to the main modulation. The output of one-shot A7U3 triggers auxiliary shaper one-shot A7U5. The output pulse width of A7U5 is also controlled by CHAL WIDTH SELECT switch S4. The output is gated through A7U2A, and modulates the rf signal generator auxiliary rf output.

(g) When the CHAL MODE SELECT switch S3 is set to CW, the outputs of gates A7U1B and A7U2A remain high and the main and auxiliary rf outputs are modulated by dc.

(h) When the ISLS pulse is selected, the output of auxiliary shaper one-shot A7U5 is inhibited by the inhibit in SLS signal from CHAL INHIB switch S15. SLS enable flip-flop A7U9 is initially cleared by the O trigger signal from the prf and delay generator. The SLS enable signal goes high and enables gate A7U8B. In modes 1, 2, 3/A, C and TEST, the first pulse (P1) at the output of main shaper one-shot A7U7 triggers SLS spacing one-shot A7U10 through gate A7U8B. Gate A7U8B is enabled for only the duration of the SLS trigger pulse. The trailing edge of the pulse clocks and sets flip-flop A7U9, which inhibits gate A7U8B. The output duration of A7U10 is determined by CHAL ISLS SPACING SELECT switch S7. The output of A7U10 triggers SLS shaper one-shot A7U11, which is enabled through inverter U4D by the inhibit in SLS signal. The output of A7U11 modulates the rf signal generator auxiliary rf output. The output duration of A7U11 is controlled by CHAL MODE SELECT switch S3. In modes 1, 2, 3/A, C, and TEST, the ISLS pulse duration in 0.8 µsec. In mode 4, the SLS pulse duration is 0.5 µsec and A7U11 is triggered by counter terms A10 and B3 through enabled gate A7U8A. For mode 4, ISLS pulse timing see FO-6.

(2) *Substitute pulse positon operation.*

(a) To substitute for pulse P1 in SIF modes and TEST, or P2, or P4 in mode 4 , CHAL SUB PULSE SELECT awitch S1 is set for the pulse to be sunstitute. This inhibits the fixed pulse triggers and enables the substitute pulse triggers (FO-5, Sheet 3).

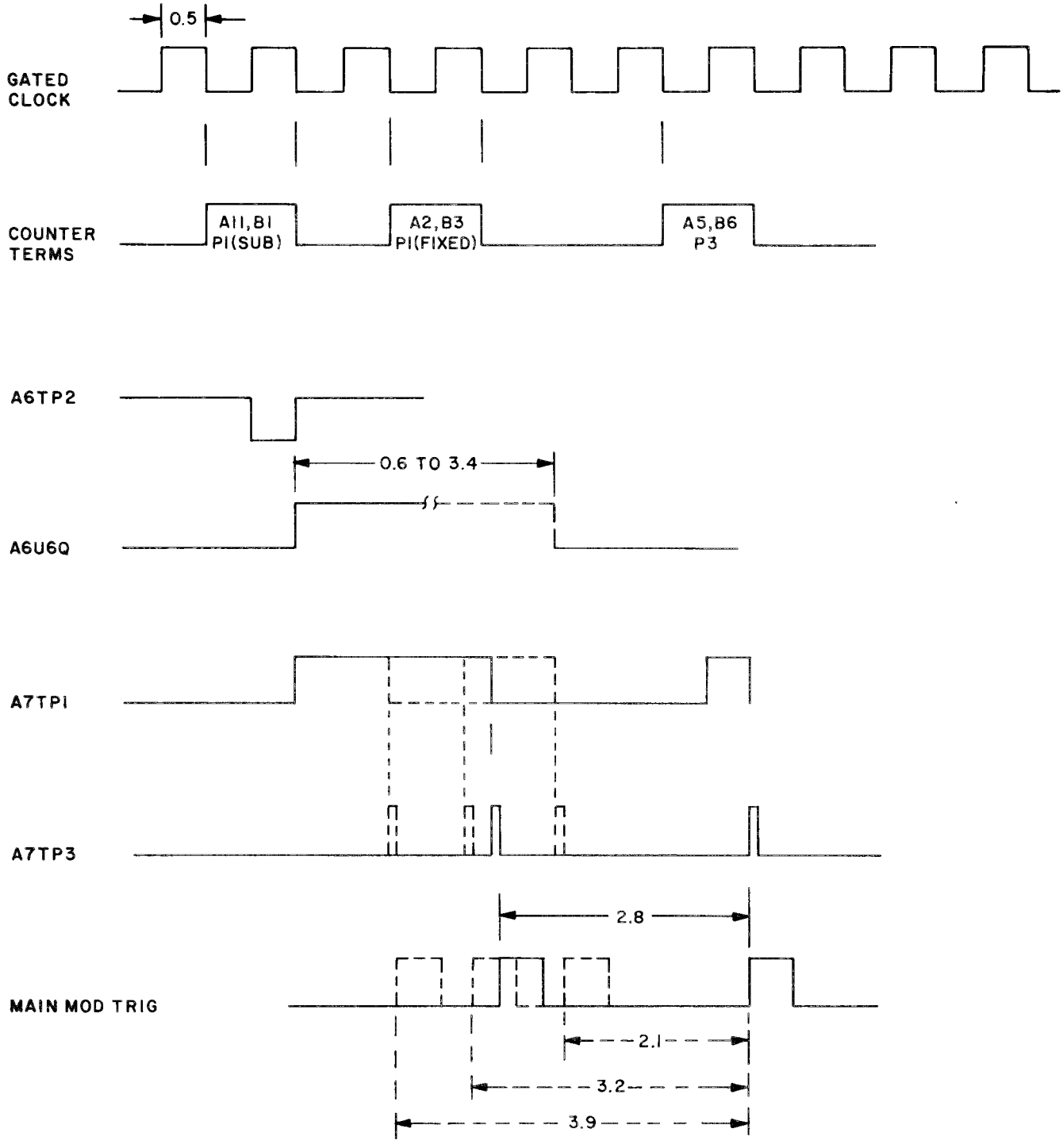
(b) If substitution is to be made for fixed pulse P1 in mode 1, the CHAL MODE SELECT switch is set to 1 and the CHAL SUB PULSE SELECT switch to SIF P1. Gates A5U13A, U13B, U14A and U14B FO-5, Sheet 1) are inhibited by the P1 inhibit signal and gate A6U2B (FO-5, Sheet 3) is enabled by the P1 substitute enable (P1 sub enable) and mode 1 enable signals. Setting CHAL SUB PULSE POSITION SELECT switch S2 to any position other than 0, enables sub pulse out gate A6U7D and determines the amount and direction P1 is shifted in relation to its nominal position. With the CHAL SUB PULSE POSITION SELECT switch S2 is set to +.2, P1 is shifted 0.2 µsec closer to P3 from its nominal position. The operation is as follows and shown in figure 2-8.

(c) Counter inputs A11 and B1 go high 2 µsec. earlier than the counter terms applied to the fixed P1 trigger gate. When this occurs, substitute trigger gate A6U2B generates a trigger pulse, gated through A6U5C by the gated clock signal which triggers sub pulse one-shot A6U6. The result is a 2.2 µsec substitute pulse trigger (sub pulse trigger) applied to gate A7U2B (FO-5, Sheet 2). The width of the sub pulse trigger is determined by the positions of the CHAL SUB PULSE POSITION SELECT switch. The sub pulse trigger triggers the main offset and auxiliary delay one-shots, which provide modulation to the rf signal generator as previously described for fixed pulse position operation. The only difference is that the mode 1 P1 and P3 pulse spacing is now 2.8 µsec instead of the nominal 3 µsec. Substitute pulse generation in the other modes functions as described for model, with the applicable gates inhibited and enabled, and pulse spacing dependent upon mode selected and setting of CHAL SUB PULSE POSITION SELECT switch S2.

b. SIF Marker Generation.

(1) The SIF markers generated in fixed frequency operation are based upon the outputs of the A- and B- counters. Each marker trigger occurs 2 µsec prior to the nominal marker position. When counter terms A6 and B7 go high, a 0 µsec marker trigger is enabled through gates A6U11A and A6U12A (FO-5, Sheet 3) and triggers marker delay one-shot A6U13. The one-shot duration is controlled by MEASUREMENT MKR PHASING control R6 and its outputs enable trigger gate A6U14A. The trigger gate output is shaped by pulse shaper A6U14B/U14C and applied through gate A6V14D and marker out amplifier A6Q2/Q3 to the MEASUREMENT MKRS OUT jack J2.

(2) The counter terms generate marker triggers at 20, 24 and 49 µsec after the 0 µsec marker trigger and in similar manner generate the 20.3 24.65, and 49.3 µsec markers, the marker triggers are delayed by one-shots A6U15, A6U16, and A6U17, as applicable.



1. ALL VALUES ARE IN USEC AND NOMINAL
   DOTTED LINES INDICATE PULSE GENERATION FOR +.9, −.2, OR −.9 POSITIONS OF THE CHAL SUB PULSE POSITION SELECT SWITCH

EL2VU008

Figure 2−8. Mode 1 substitute pulse operation timing diagram

(3) In swept frequency mode, gate A6U7A is enabled, and sweep frequency markers (sweep freq markers) from the rf signal generator are applied through gate A6U7A to the marker output circuits. Gate A6U14C is disabled by the FIXED ENABLE to disable the SIF markers.

c. *Mode 4 Interface.*

(1) The mode 4 interface provides a 3-pulse reply signal 200 µsec after receipt of a mode 4 enable trigger from the transponder, and disparity signals, when selected by CHAL INHIBIT switch S15. In addition the mode 4 interface provides a resistive termination for the mode 4 challenge video from the transponder under test. Timing for the 3-pulse reply is shown in figure 2-9.

(2) The mode 4 enable trigger signal, received

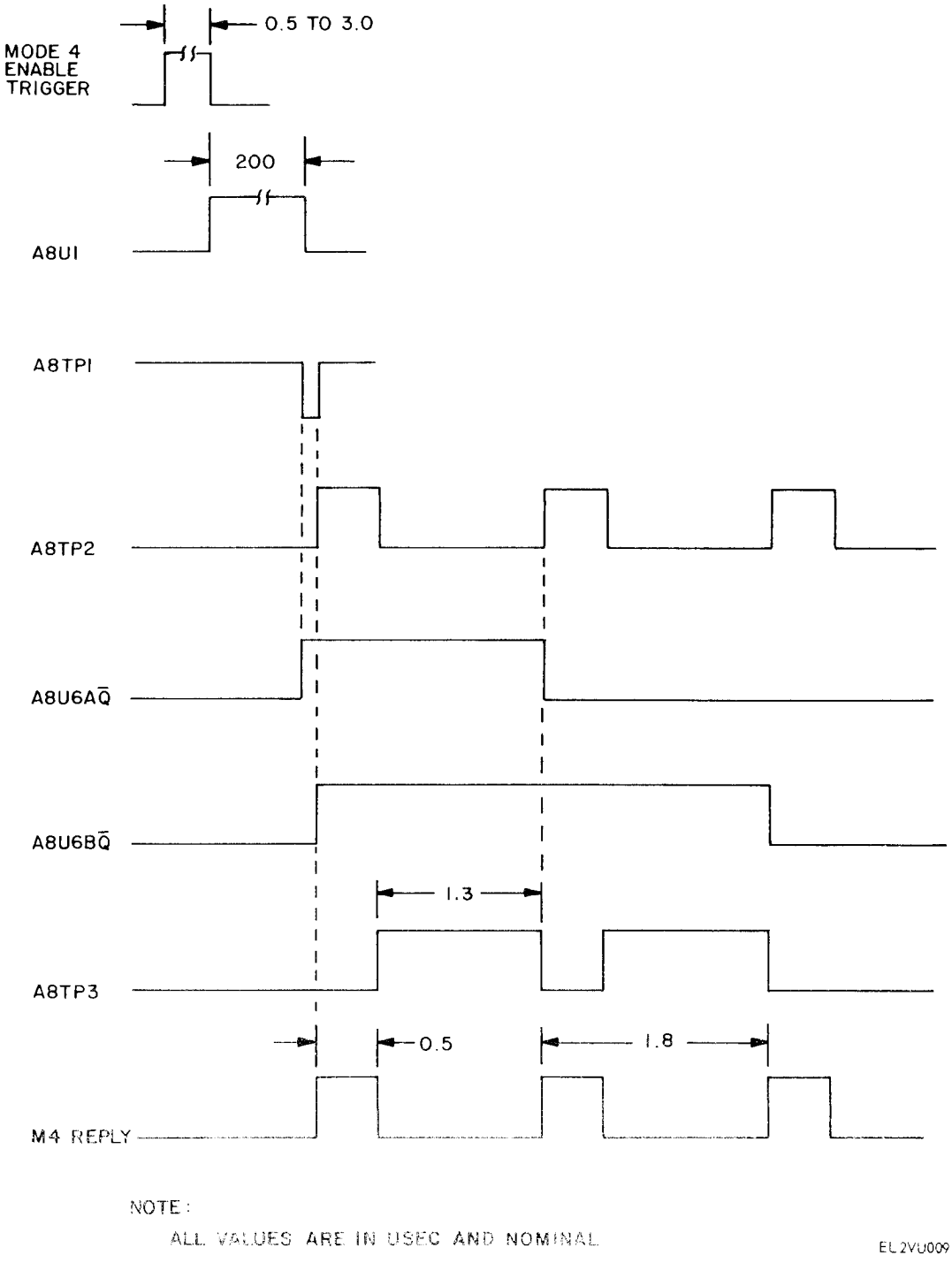


Figure 2-6. Mode 4, three-pulse reply timing diagram.

from the. transponder under test, is buffered by amplifier A8Q1 (FO-5, Sheet 2) and triggers M4 reply delay one-shot A8U1. When one-shot A8U1 times out, it clears 3-pulse counter flip-flop A8U6A and triggers M4 reply generator one-shot A8U4 which generates the M4 reply pulses. The trailing edge of the first reply pulse triggers reply pulse spacing one-shot A8U5 which establishes the spacing between the reply pulses. The trailing edge of the 1.3 µsec pulse clocks and sets flip-flop A8U6A and triggers one-shot A8U4 for the second reply pulse. The trailing edge of the second reply pulse again triggers one-shot A8U5, and the trailing edge of this 1.3 µsec pulse clocks and sets 3-pulse counter flip-flop A8U6B and triggers one-shot A8U4 for the third reply pulse. With flip-flop A8U6B set, one-shot A8U5 is inhibited, limiting the mode 4 reply to three pulses, 0.5 µsec wide, and spaced 1.8 µsec. apart from leading edge to leading edge. When the next mode 4 enable trigger signal is received, the operation is repeated as described.

(3) When CHAL INHIB switch S15 is set to ISLS ON, the mode 4 reply is inhibited by the inhibit in SLS signal and the mode 4 enable trigger input triggers M4 disparity delay one-shot A8U7. When one-shot A8U7 times out, it triggers disparity pulse generator one-shot A8U11 and 0.5 µsec disparity pulse is generated.

(4) When CHAL INHIBIT switch S15 is set to DISPARITY (MOM), the mode 4 reply is inhibited by the inhibit in disparity signal and gate A8U9B is enabled through inverter A8U8A. Counter terms A2 and B5 correspond to the pulse in the 66 µsec position of the mode 4A or B challenge word. These counter terms generate a disparity pulse that corresponds to the pulse missing from the mode 4 challenge word.

(5) Pressing BIT (MOM) switch S16 during self-test enables gate A8U9A. Counter terms A8 and B1 simulate a mode 4 enable trigger and initiates a 3-pulse reply.

(6) Normally, the transponder receiver demodulates the challenge rf and when a mode 4 challenge is decoded, the transponder outputs the challenge word to the mode 4 computer. In the absence of the mode 4 computer, the mode 4 challenge video is terminated by resistor A8R1.

2-6. RF Signal Generator. (FO-7)

The following is a description of the overall rf signal generator operation. This is followed by a more detailed description of rf generator A11, and dual modulator A16.

a. Fixed Frequency Operation.

(1) In fixed frequency operation, a 1030 MHz rf signal is developed by rf generator A11. The rf signal level is from +17 to +21 dBm, and is applied to dual modulator A16 thru circulator HY1. The main modulator video (main mod video) and auxiliary modulation video (aux mod video) signals from the video generator modulate the main mod rf and auxiliary mod rf outputs respectively.

(2) The main mode rf is applied through 9 dB coupler, MAIN ATTEN control AT1, 20 dB coupler DC1 and attenuator AT3 to the RF IN/OUT MAIN jack. Coupler DC2 combines the modulated SLS pulse with the main mod rf signal. Coupler DC2 also blocks dc between the main output of dual modulator A16 and the rf output of the test set. The MAIN ATTEN control AT1 adjusts the rf output level from -10 to -99 dBm. Coupler DC1 couples an input rf signal from the RF IN/OUT MAIN jack to the receiver.

(3) When CHAL INHIB switch S15 is in any position except ISLS ON, the auxiliary mod rf signal is applied through AUX ATTEN AT2, rf switch S21, adjustable pad AT5, attenuator AT9, multicoupler DC3, and attenuator AT4 to the RF IN/OUT AUX jack. The AUX ATTEN control varies the output of the RF IN/OUT AUX jack from -10 to -90 dBm.

(4) Setting CHAL INHIB switch S15 to ISLS ON energizes rf switches S20 and S21. The auxiliary mod rf signal, which for this condition is the SLS pulse, is routed through the rf switches and combined with the main mod rf signal by coupler DC2.

b. Swept Frequency Operation. In swept frequency operation, rf generator All generates either a narrow or wide sweep rf signal, and frequency markers. The rf sweep width is selected with SIG GEN FCTN switch S17, the RF output is in sync by the sweep trigger output from sweep generator and timing markers (A9). Setting SIG GEN FCTN switch to SWP ± 5 MHZ, generates a narrow sweep rf signal which varies from 1025 to 1035 MHz at a 800 Hz rate. Setting the switch to SWP ± 20 MHZ, generates a wide sweep rf signal which varies from 1010 to 1050 MHz at a 250 Hz rate.

(1) *Narrow sweep operation.*

(a) Setting the SIG GEN FCTN switch to SWP ± 5 MHZ, applies -12v to gate A3U5A, and ground to sweep rate generator A9U1D which provides the ramp trigger signal to the rf source. Crystal Yl, Ql, and Q2 provides a clock to counters A9U2, U3, and U5 to the prf and delay generators. Sweep trigger is generated by counters A9U2A, U7, U10, U11, and U8. Potentiometer A11A1R80 sets the narrow sweep duration of the sweep rate generator U11B.

(b) The sweep rate generator A11A1 provides an adjustable bias and ramp to the RF source A11A2. The sweep ramp signal initiates the sweep rf output of rf source A11A2. The duration and symmetry of the sweep ramps signal is adjusted by potentiometers A11A1R80 and A11A1R74 respectively. Potentiometer A11A1R73 adjusts the sweep ramp output voltage. The sweep sync clock signal, applied to the marker/ramp generators, triggers the oscilloscope

sweep at the start of each rf sweep cycle, triggers the delay trigger circuit, initiates generation of the 0.1, 1.0, and 10.0 µsec timing markers, and also initiates generation of the challenge word. It also causes cycling of the frequency marker generations which enable the frequency markers to be displayed on each sweep. The rf source output is applied to the RF IN/OUT jacks as previously described.

(2) *Wide sweep operation.* Setting the SIG GEN FCTN switch to SWP ± 20 MHZ applies -12v to gate A3U5A, and ground to A9U1E, the sweep rate generator timing network. Potentiometer A11A1R79 sets the wide sweep duration of the sweep rate generator U11B and R66 adjusts the symmetry. Bias voltage is not applied to A11A1Q4 permitting a full fixed slope duration for wide sweep operation. The remainder of the operation is as previously described.

c. R.F. Generator A11.

(1) *Primary frequercy loop A11A2A1 (FO-7), frequency control of the power oscillator.* In the sweep mode of operation, the phase detector U4 accepts the POS GATE input signal from A11 marker ramp generator, coupled with 12.875 MHZ oscillator Yl, U5A, and U5D. Phase detector U4 output is applied to sample and hold U3. This error signal is coupled with the ramp in and applied to CR1 to the voltage controlled oscillator U2 The resultant ramp voltage output is applied to phase detector U4. The phase detector amplifier controls the sweep rate of the swept frequency rf signal. When SIG GEN FCTN switch is set to FIXED FREQ, the POS GATE OUT signal from A11A1 does not enable AND gate U5B.

(2) *Power oscillator A11A2A2 is the source of rf in the unit.*

(a) In the sweep mode of operation, the phase detector U1 provides an error signal to integrator U2. The output ramp slope of U1 is controlled by R1, R2 and C3. The integrator U2 output is applied to (varactor) diode CR3, which is tuned to the eightieth harmonic of the input frequency which is 12.87500 MHz. Capacitor C19 is tuned to the eightieth harmonic of the input rf signal, coupled through Q2 to coupler DC1. The 1030 MHz rf signal, which is broad-tuned for a 1010 to 1050 MHz bandpass is coupled thru DC1 to the divide by eighty counter U3, U4, and U5, which is then coupled thru U6A to phase detector U1.

(b) Output signal of 12.87500 MHz from U6A is sent to inverter U6B to A11A2J2. The signal at A11A2J2 is coupled to A11A1J1 marker generator board.

(c) ALC is provided for rf leveling through coupler DC1 through detector diode CR4 to operational amplifier U7. The dc bias controls CR4 condition and effectively the rf output level coupled to jack J2. Potentiometer R26 and A11A1R2 are set for an rf output of +19 dBm at output to dual modulator A16, and +5 dBm LO OUT jack J4 to rf BIT/MIXER A15.

(3) *Marker ramp genertor A11A1 provides the rf markers and ramp for the primary loop.*

(a) Crystal frequency marker generator A11A1 generates markers corresponding to 1010, 1025, 1027, 1029, 1030, 1031, 1033, 1035, and 1050 MHz. The marker generator is enabled on receipt of each GATE IN signal and RAMP IN signal triggered by sweep generator and triming markers from A9 through ramp generator.

(b) Each marker generator has one crystal. The crystal outputs are rectified within each generator and applied to its respective threshold amplifier. Potentiometers R6, R11, R16, R21, R26, R31, R36, R41, and R46 establish the marker output frequency, and the markers are applied through quad line receivers A11A1U3, U4, and U5 to one-shot U6A and U6B, and the outputs are combined at the junction of CR10 and CR11 and seen at MARKERS OUT jack after being isolated by emitter follower Q2.

(c) Initially when an input trigger is generated by sweep generator and timing markers A9 to marker ramp generator A11A1 the Q output of A11A1U11 B is applied to one-shot U7, the one-shot output is applied through inverters U3, U4, and U5 pin 4, inhibiting the gate for an additional 170 µsec to prevent the output of spurious signals.

d. Dual Modulator A16.

(1) Dual modulator A16 contains main and auxiliary rf modulators. The main mod video from the video generator is applied through inverter A1U1A and A1U1B to driver amplifier Al Q7/Q8, and through inverter A1U1A to driver amplifier A1 Q5/Q6. The push-pull driver applies bias to the main modulator and the rf input from rf generator All is effectively modulated by the main mod video. The main mod rf output is applied to 9 dB coupler DC2 as previously described. In the absence of the main mod video, the main modulator is biased-off, and there is no main mod rf output. Potentiometer R40 sets the plus voltage level of the driver stage to provide the best pulse shape and pulse/cw power balance. The operation of the auxiliary modulator is as described for the main modulator.

(2) When the CHAL MODE SELECT switch is set to CW, the main mod video and auxiliary mod video inputs remain high holding the main and auxiliary modulators in the on condition.

2-7. Receiver (FO-8)

a. Inputs to the RECEIVER (nominally 1090 MHz) can be acted upon in two ways; they can be detected and applied directly to the measurement section, or mixed with a local oscillator signal to produce an i-f

signal which is amplified and applied to the measurement section. In fixed frequency operation normally the input signal is detected only, and measured for peak power and pulse fidelity. In swept frequency operation normally the input signal is mixed, amplified, and detected and measured for frequency. Signals between -12 and +3 dBm are applied to LOW POWER IN jack J1 and coupled through 9 dBm mult/coupler DC3 to rf BIT/MIXER A15. Signals between +5 and +25 dBm are applied through the accessory attenuator to LOW PWR IN jack J1.

b. The detector/amplifier output is the fidelity and power video signal which is applied to the measurement section. The 1030 MHZ cw rf input signal from the rf source (LO) is applied to J2 of rf BIT/MIXER A15 and combined with the incoming signal (RF). The l090 MHz signal under test (RF), and the 1030 MHz cw acting as a local oscillator are mixed and the resultant (IF) is applied through rf BIT/MIXER A15 to filter/amplifier A14. The rf BIT/MIXER output is 60 MHZ i-f signal when the local oscillator and the unknown frequency are exactly 60 MHz apart. Since in swept frequency operation the local oscillator is sweeping, a 60 MHZ difference exists at some point in the sweep. The 60 MHz signal is applied to i-f amplifier A14 and the amplified signal is applied to the measurement section. The rf signal generator output can also be coupled into the LOW PWR IN jack to self-test the internally generated rf for frequency, pulse fidelity and peak power characteristics.

c. Signals above 100W (+50 dBm) are applied to either RF IN/OUT MAIN or AUx jack. The input to be demodulated is selected with RF IN/OUT DEMOD switch S18. With the RF IN/OUT DEMOD switch set to MAIN, inputs applied to the RF IN/OUT MAIN jack are coupled through attenuator AT3, 20 dB coupler DC1, to mult/coupler DC3. From this point the operation is as described for the LOW PWR IN jack. With the RF IN/OUT DEMOD switch set to AUX, the RF IN/OUT AUX jack is coupled through attenuator AT4 to coupler DC3. The operation is them as previously described.

d. During swept frequency operation pressing BIT (MOM) switch S16 activates rf bit A15. The 1090 MHz rf generator is activated. The rf is combined with the rf input signal from the rf source. The resultant 60 MHz i-f signal is processed as previously described. The BIT (MOM) switch thus provides a check the 60 MHz i-f and measurement circuitry, rf sweep frequency markers and also rf BIT/MIXER A15.

2-8. Measurement Section.
(FO-9)

The inputs to the measurement section from the receiver and prf and delay generator, are converted to prf or power indications which are displayed on MEASUREMENT meter M1. Frequency measurement signals are also made available at MEASUREMENT DEMOD VID OUT jack J3 for display on an oscilloscope.

a. PRF and POWER Measurements.

(1) When MEASUREMENT FUNCTION SELECT switch S10 is set to PRF CHAL, gate A8U10B is enabled. The 0 trig signal from the prf and delay generator is applied through gates A8U10B and A8U10D to 99 µsec blanking one-shot A10U1. The prf count trigger triggers one-shot A10U1, which in turn triggers prf pulse shaper one-shot A10U2. The pulse from one-shot A10U2 is integrated by amplifier A10U3 into a dc level which is applied through amplifier A10Q8/Q9 to MEASUREMENT meter M1. MEASUREMENT PRF RANGE switch S9 selects the range multipler time constant for the prf range to be measured.

(2) When MEASUREMENT FUNCTION SELECT switch S10 is set to PRF REPLY, gate A8U10C is enabled. The amplified fidelity and power video signal from the receiver is applied to MEASUREMENT DEMOD VID OUT jack J3 for oscilloscope display. The video amplifier output is applied to MEASUREMENT DEMOD VID OUT jack J3 for oscilloscope display. The pulse shaper output is gated through A8U10C, triggering one-shot A10U1, which triggers one-shot A10U2, applying a pulse to MEASUREMENT meter M1. The 99 µsec diration of one-shot A10U1 allows only the first pulse of each reply pulse train to be counted. Therefore, each pulse group to be measured in converted into a single one-shot pulse which is independent of the number or width of the pulses being measured. The dc level applied to the meter is proportional to the prf of the replay signal.

(3) When MEASUREMENT FUNCTION SELECT switch S10 is set to PWR, an adjustable signal from MEASUREMENT DEMOD VID LEVEL control R7 is applied to amplifier A10Q1. For power measurements, the MEASUREMENT DEMOD VID LEVEL control is adjusted until the fidelity and power video signal at the MEASUREMENT DEMOD VID OUT jack is 1-volt in amplitude. The voltage necessary to maintain this 1-volt reference is proportional to the rf power level at the input of detector AR2, and is therefore read out directly on MEASUREMENT meter M1 as peak power.

b. Frequency Measurement. When MEASUREMENT FUNCTION SELECT switch S10 is set to FREQ, + 12v activates i-f detector A10Q5. The 60 MHz i-f freq meas video signal is detected by A10Q5, amplified by video amplifiers A10Q1/Q4 and applied to the MEASUREMENT DEMOD VID OUT jack for display. The position of the displayed peaked video signal in relation to the swept frequency markers determines the frequency of the original signal.

2-9. Power Supply.
(FO-10)

a. General

(1) The power supply converts 115v, 45/66 Hz 380/420 Hz primary power into regulated dc outputs of +28, +12, -12, and +5 volts. The ac input power is fuse-protected against overload, and a power dc fault sensor circuit detects and gives an indication of an over/under voltage condition of any dc supply.

(2) The 115 vac primary power is applied through POWER connector J1, EM1 filter FL1/FL2, POWER ON/OFF switch S19, and POWER 1 AMP fuse F1 to power supply PS1. When power is applied, POWER indicator XDS1 lights. If fuse F1 opens, the fuseholder neon lamp lights. If a dc supply over/under voltage condition exists, POWER DC FAULT indicator XDS2 lights.

b. Power Supply PS1. The primary power input to power supply PS1 is applied through EM1 filter L1/L4 to the primary of transformer T1. Transformer T1 provides a secondary output for the power dc fault sensor, and the +28, +12, and +5 volt outputs. The -12 volt output is derived from the same secondary as the +12v.

(1) *Power dc fault sensor.* The secondary output of transformer T1 is rectified by bridge rectifier A1CR2/CR3, and provides a voltage to Q1 and for panel lamp. Each power supply output is monitored by an over/under voltage sensor A1U2 and A1U3. Each over/under voltage sense output goes to lamp driver A1Q1/Q2. If an over/under voltage condition is sensed for any dc output, lamp driver A1Q1/Q2 supplies a ground for POWER DC FAULT indicator XDS2.

(2) *+28v output.* The secondary voltage of transformer T1 is rectified by CR1/CR2, and applied to series regulator Q1. Voltage reference amplifier U1 controls current flow through the series regulator, maintaining the +28v output at a constant level. Over/under voltage sensor U3 monitors the +28v output, and if an over/under voltage condition occurs, the sensor output drives the output of the lamp driver A1Q1/Q2 low, and the POWER DC FAULT indicator lights.

(3) *+12v output.* The secondary voltage of transformer T1 is rectified by bridge CR3/CR6, and applied to series regulator Q2. Voltage sense amplifier U4 controls current flow through the series regulator, maintaining the +12v output at a constant level. Over/under voltage sensor U2 monitors the +12v output, and if an over/under voltage condition occurs, the sensor output drives the output of lamp driver A1Q1/Q2 low, and the POWER DC FAULT indicator lights.

(4) *-12v output.* The secondary voltage of transformer T1 is rectified by bridge CR3/CR6, and applied to series-regulator Q3. Voltage reference amplifier U5 controls current flow through the series regulator, maintaining the -12v output at a constant level. Over/under voltage sensor U2 and U3 monitors the -12v output, and if an over/under voltage condition occurs, the sensor output drives the output of lamp driver A1Q1/Q2 low, and the POWER DC FAULT indicator lights.

(5) *+5 output.* The secondary voltage of transformer T1 is rectified by CR7/CR8, and applied to series regulator A2Q1/Q2. Voltage sense amplifier A1U6 controls current flow through the series regulator, maintaining the +5v output at a constant level. Over/under voltage sensor A1U2 monitors the + 5v output, and if an over/under voltage condition occurs, the sensor output drives the output of lamp driver A1Q1/Q2 low, and the POWER DC FAULT indicator lights.

CHAPTER 3

GENERAL SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Level of Maintenance.

This chapter provides general support maintenance procedures for the test set. Included in this chapter are sections covering: troubleshooting, removal and replacement; adjustment and alignment; repair, and general support testing.

3-2. Maintenance Forms and Records.

Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750.

3-3. Tools and Test Equipment.

Tools and test equipment required for general support maintenance. Repair parts, special tools, special test equipment, and accessories issued with or prescribed for use by the operator for the AN/APM-305A are listed in the Maintenance Allocation Chart, Appendix D Of TM 11-6625-2611-12.

3-4. Equipment Preparation for Maintenance.

The test set should be prepared for maintenance in the following procedure.

a. Test Set Preparation for General Support Maintenance. To prepare the test set for maintenance, connect power cable from test set POWER connector to 115 vac power source. Set the POWER ON/OFF switch to the ON position. Position the remaining controls as indicated in table 3-1.

Table 3-1. Test Set, Control Settings

Controls	Settings
MEASUREMENT PRF RANGE switch	XIK
MEASUREMENT FUNCTION SELECT switch	PRF CHAL
MEASUREMENT DEMOD VID LEVEL	Mid-range
MEASUREMENT MKR PHASING control	Mid-range
CHAL SUB PULSE SELECT switch	SIFP1
CHAL SUB PULSE POSITION SELECT switch	0
CHAL SUB PULSE POSITION VARY control	Mid-range
CHAL MODE SELECT switch	1
CHAL WIDTH SELECT switch	0.80
CHAL WIDTH VARY control	Mid-range
CHAL ISLS SPACING SELECT switch	0
CHAL ISLS SPACING VARY control	Mid-range
CHAL INHIB switch	OFF
CHAL AUX MOD DLY control	Fully counterclockwise
PRF SELECT RANGE switch	XIK
PRF SELECT MULT control	5.0
PRF SELECT switch	X1
SCOPE TRIG/FREQ MEAS DELAY (μSEC) RANGE switch	OFF
SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control	5.0
SUPPR switch	ON
AUX TRIG switch	ON
MAIN ATTEN control	-10
AUX ATTEN control	-10
RF IN/OUT DEMOD switch	MAIN
SIG GEN FCTN switch	FIXED FREQ

Section II. TROUBLESHOOTING

3-5. General Troubleshooting Instructions.

Troubleshooting at the general support maintenance level of the test set includes all the techniques outlined for organizational maintenance, and any special or additional techniques required to isolate a defective part. The maintenance procedures are not complete in themselves, but supplement those described in TM 11-6625-2611-12. The systematic troubleshooting procedure begins by performing the performance test procedure in table 3-2. When an abnormal indication is noted when performing the performance test procedure reference is made to the corresponding malfunction in table 3-3 to sectional troubles to a particular functional unit of the test set, and then to localize the trouble to a component of the functional unit unless the functional unit is replaced and later repaired at a higher level maintenance facility. Test point locations are shown in figure 3-1. Parts location information is provided in figure 3-2 thru 3-10. Wiring diagram information and cable diagrams are provided in figure FO-13. Color codes for resistors, inductors, and capacitors are provided in figure FO-1.

3-6. Organization of Troubleshooting.

a. General. The first step in troubleshooting the test set is to sectionalize the fault (tracing the fault to a major functional unit). The second step is to localize the fault (tracing the fault to a defective part within the unit). Some fault, such as burned-out resistors, arcing, and shorted transformers can often be located by sight, smell, and hearing. The majority of faults, however, must be isolated by performing the performance test procedure in table 3-2.

b. Sectionalization. For ease of troubleshooting, the equipment may be thought of as consisting of functional entities, each related electrically but categorized separately by the function performed. The first step in troubleshooting is to locate the function, or functions, at fault by the following methods:

(1) Visual inspection. The purpose of the visual inspection is to locate faults without testing or measuring the circuits. All visual signs should be observed and an attempt made to sectionalize the fault to a particular function.

(2) *Performance test.* The performance test (table 3-2) frequently indicates the general location of trouble. In many instances the test will help in determining the exact nature of the fault.

c. *Localization.* The tests listed in the following paragraphs will aid in localizing the trouble. First, localize the trouble to a single function, and then isolate the trouble within that circuit by waveform, voltage, resistance, and continuity measurements.

(1) Troubleshooting chart. When used with the performance test procedure, voltage, resistance, continuity measurements, and the waveform diagram, the troubleshooting information in table 3-2 will aid the technician in localizing troubles to a component part. Defective components identified by performing corrective action are replaced with a known reliable component unless repair or other disposition is noted. The corrective action column references data tables, if required, for checking components; otherwise, refer to schematics and wiring diagrams when performing checks. The referenced data items and test procedure steps will allow malfunction symptoms discovered during performance of the test procedure to be easily referenced in the troubleshooting chart.

(2) Voltage and resistance measurements. A multimeter is used for taking voltage and resistance measurements on the chassis. Voltage and resistance measurements are listed in chart 3-1.

CAUTION

When making voltage measurements of transistors, use tape or sleeving to insulate the test probe except for the extreme tip, to prevent accidental shorting of the test probe to the chassis (even a momentary short circuit can damage the transistor).

(3) *Continuity checks.* Routine continuity checks between various points in the circuitry can be made using multimeter and the wiring diagrams.

(4) lntermittent *troubles.* When troubleshooting, the possibility of intermittent troubles should not be overlooked. This trouble can often be made to appear by tapping or jarring the equipment. Check wiring and connections.

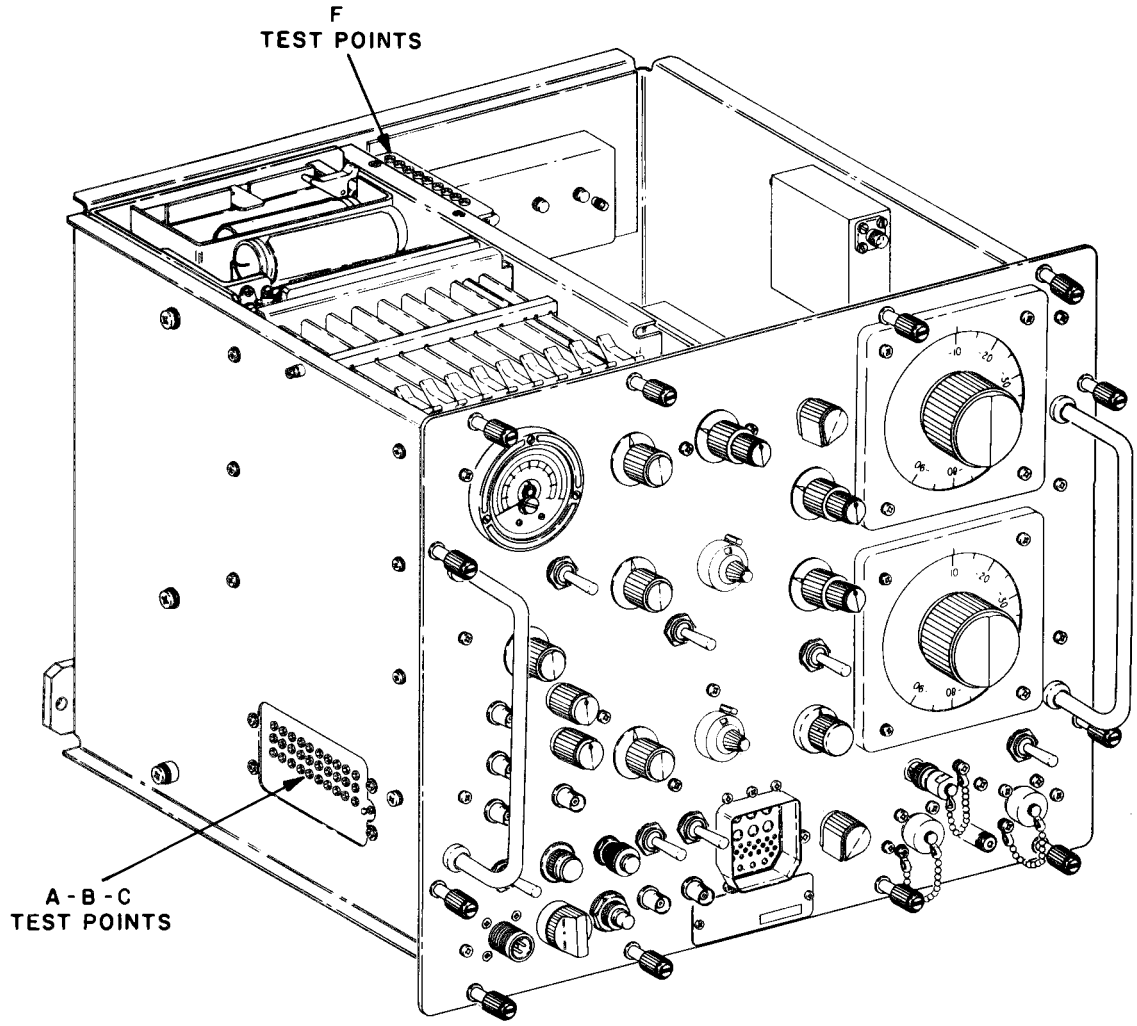
3-7. Interunit Troubleshooting.

a. Defective Signal Monitoring. Failure to monitor a selected voltage or signal may be caused by defective external test equipment. If an operational check fails to sectionalize trouble to a defective major functional area, follow the procedures given in (1), (2), and (3) below.

(1) *External test equipment check.* All external test equipment should function properly. Perform operational checks on each unit of external test equipment as described in the applicable test equipment manual.

(2) *Active circuits.* If any of the transistor or diode circuits are suspected of causing malfunction, isolate the trouble by using voltage and resistance measurements with external test equipment.

(3) *Controls.* To verify that all controls are functioning properly, perform continuity measurements



TP IDENTIFICATION

	A	SOURCE	B	SOURCE	C	SOURCE	F	SOURCE
1	RAW PRF TRIG	A1-15	SUB PULSE TRIG	A6-37			MOD MAIN−	A16E16
2	RAW DELAY TRIG	A2-48	TEST MODE TRIG	A2-10	CLOCK	A9-15	MOD MAIN+	A16E18
3	FIXED ENABLE	A3−47	AUX MOD VID	A7-25	SWEEP TRIG	A9-3	MOD AUX−	A16E11
4	COUNTER INITIALIZE	A3-22	MAIN MOD VID	A7-12	DET INPUT	A10-39	MOD AUX+	A16E13
5	0 TRIGGER	A3-24	PRF COUNT	A8-31	DET IF	A10-24	VIDEO OUT	P6-7
6	GATED CLOCK	A3-18			50% VID WIDTH	A10-5	RAMP OUT	P5-13
7	A11	A4-13			IF INPUT	A10-26	POS GATE	P2-8
8	B7	A4-35						
9	CHAL WORD CODE GATE A/B	A5-10					+12VDC	TB3-E5
10					IF AMPL OUT	AR14-E2	A15 DET BIAS	A15-FL2

EL2VU010

Figure 3-1. Test set location of test points

while the controls are rotated through each position.

b. *Checking Cable Assemblies.* All interconnecting cable assemblies should be checked for signs of insulation deterioration and for opens or shorts near the connectors. Check connectors for bent or deformed pins and for signs of arcing.

Voltage and resistance chart

a. Transistor terminal voltages.

Transistor or diode	DC voltage			Transistor pin locations
	Base to GND	Emitter to GND	Collector to GND	
PS1Q1	+6.4 vdc	+8.0 vdc	+5.3 vdc	See figure FO–14
PS1Q2	+5.9 vdc	+5.3 vdc	+6.4 vdc	
PS1Q3	+0.0 vdc	0 vdc	+5.0 vdc	

b. Transformer T1 pin voltages (multimeter connected between pins indicated)

1 and 2	3 and 5	6 and 8	9 and 11	12 and 14
115 vac (line)	50 vac ±10%	50 vac ±10%	24 vac ±10%	12 vac ±10%

c. Transistor and diodes resistances (in circuit resistances with multimeter set to RX10) with PS1A1 Board removed.

Connector	Pin	To	Pin	Resistance
J2	X		W	<4 ohms
	X		GND	infinite
	L		J	<1 ohm
	L		GND	>10K ohm
	H		GND	>10K ohm
	D		GND	>10K ohm
	S		GND	>10K ohm

Table 3-2. Performance Test Procedures

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal, see Table 3–3
	Oscilloscope	Test set			
			Power Supply Test		
1	Connect oscilloscope	Set up test set as described in paragraph 3–4*a*	Connect oscilloscope to test set as shown in figure 3–22. Check POWER indicator.	POWER indicator illuminates.	Malfunction 1 and Malfunction 2
2			Check POWER DC FAULT indicator.	POWER DC FAULT indicator is extinguished.	Malfunction 3
3			Press POWER DC FAULT indicator.	POWER DC FAULT indicator illuminates.	Malfunction 8
			PRF Generator and PRF Measuring Section Test		
4			Adjust PRF SELECT MULT control until meter indicates 9.0 Hz scale. Observe measurement meter.	PRF SELECT RANGE and MULT controls indicate prf is 8,100 to 9,900 Hz.	Malfunction 9
5		PRF SELECT RANGE switch X100 MEASUREMENT PRF RANGE switch X100	Adjust PRF SELECT MULT control until meter indicates 10.0 on Hz scale. Observe measurement meter.	PRF SELECT RANGE and MULT controls indicate prf is 900 to 1100 Hz.	Malfunction 9

Table 3-2. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal, see Table 3-3
6		PRF SELECT RANGE switch X10 MEASUREMENT PRF RANGE switch X10	Adjust PRF SELECT MULT control until meter indicates 10.0 on Hz scale.	PRF SELECT RANGE and MULT controls indicate prf is 90 to 110 Hz.	Malfunction 9
7		PRF SELECT switch X 1/2	Observe MEASUREMENT meter.	Meter indicates 45 to 55 on Hz SCALE.	Malfunction 14
			Timing Marker Test		
8		Set up test set as described in paragraph 3-4a, and fig. 3-22. Except remove video cable from MKRS OUT jack J2, and connect to TIMING MKRS jack J8.	Observe three sets of markers. Each set will be of different amplitude and spacing.	Three sets of markers are present.	Malfunction 15
9			Measure spacing between leading edge of the lower amplitude set of pulses.	Pulses are spaced 0.1 µsec. ≥ 0.5 volts amplitude.	Malfunction 15
10			Observe second set of pulses. (Amplitude level more than previous pulses but less than the third set of pulses.)	Pulses are spaced 1.0 ±.02% µsec. >0.5 volts amplitude.	Malfunction 15
11			Observe third set of pulses with first, and second set within third set.	Pulses are spaced 10.0 ±.02%, >0.5 volts amplitude.	Malfunction 15
			SIF Generator Test		
12		CHAL MODE SELECT switch C	Observe two pulses are present on DISPLAY A with TIMING MKRS on DISPLAY B.	Two pulses are present	Malfunction 14
13			Measure spacing between leading edges of pulses on DISPLAY A.	Pulses are spaced 21.0 µsec ±0.05 µsec	Malfunction 22
14		CHAL MODE SELECT switch 1	a. Observe number of pulses.	a. Two pulses are present.	a. Malfunction 14
15		CHAL MODE SELECT switch 2 MEASUREMENT FUNCTION SELECT switch PRF REPLY	b. Observe MEASUREMENT meter.	b. Meter indicates prf is 4500 to 5500 Hz.	b. Malfunction 53
16		CHAL MODE SELECT switch 3/A	Observe number of pulses.	Two pukes are present.	Malfunction 22
17		CHAL MODE SELECT switch TEST	Observe number of pulses.	Two pulses are present.	Malfunction 25
18		CHAL MODE SELECT switch 4A PRF SELECT X 1/2	Observe number of pulses.	28 pulses total displayed.	Malfunction 26

Table 3-2 Performance Test Procedure-Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal, see Table 3-3
	Oscilloscope	Test set			
19			Measure spacing between first four pulses and last two pulses.	First four pulses ar each spaced in 2.0 µsec ±0.07 µsec in crements. Last tw pulses are spaced 3. µsec ±0.07 µsec.	Malfunction 26
20		CHAL MODE SELECT switch 4B	Observe number of pulses.	28 pulses total displayed	Malfunction 27
			Dual 3/A Mode Operation Test		
21		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X40 CHAL MODE SELECT switch DUAL 3/A PRF SELECT RANGE switch X100 PRF SELECT Xl.	Disconnect cable from test set MEASUREMENT SCOPE TRIG OUT jack and connect to AUX TRIG OUT jack. Observe that display consists of two challenges. Vary SCOPE TRIG/FREQ MEAS DELAY (uSEC) MULT control.	Spacing between chal lenges train vary with SCOPE TRIG/FREQ MEAS (µSEC) MUL control from 40 to greater than 400 µsec	Malfunction 28
			SIF Marker Test		
22		CHAL MODE SELECT switch 1 SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch OFF	Disconnect cable from test set AUX TRIG OUT jack and connect to MEASURE. MENT SCOPE TRIG OUT jack. Disconnect cable from timing MRKS jack J8 and connect to MRKS J2. Observe markers on oscilloscope B INPUT	Four markers are displayed on B INPUT	Malfunction 30
23			Using oscilloscope DIV DELAY control, measure spacing between second pulse on A INPUT and first pulse on B input while varying. Test set MEASUREMENT MKR PHASING control.	First marker on E INPUT moves at least from 2 to 4 µsec from second pulse on A INPUT.	Malfunction 30
24		PRF SELECT RANGE X1K	Disconnect cable from DEMOD VID jack J3 and connect to TIMING MRKS J8. Measure spacing between leading edges of first and second markers on B INPUT. Use MEASUREMENT MKR PHASING control to align pulse on DISPLAY B with TIMING MKRS on DISPLAY A.	Markers are spaced 20.30 µsec ±0.02 µsec	Malfunction 31

Table 3-2. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal, see Table 3-3
25			Measure spacing between leading edges of first and third markers on B INPUT.	Markers are spaced 24.65 µsec ±0.02 µsec	Malfunction 31
26			Measure spacing between leading edges of first and fourth markers on B INPUT	Markers are spaced 49.30 µsec +0.02 µsec	Malfunction 31
		Delay Operation Test			
27		PRF SELECT MULT control 1.0	Note position of first marker.	Not applicable.	Not applicable.
28		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X0.4 SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 5.0	Markers shift toward beginning of sweep. Vary SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control.	Marker shifts when SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control is varied.	Malfunction 28
29		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X4	Markers shift toward beginning of sweep. Vary SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control.	Marker shifts when SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control is varied.	Malfunction 28
30		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X40	Second set of markers shift toward beginning of sweep. Vary SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control.	Markers shift when SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control is varied.	Malfunction 28
31		SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 1.0 SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X400	Markers shift toward beginning of sweep. Vary SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control	Markers shift when SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control is varied.	Malfunction 28
		SIF Pulse Width Test			
32		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch OFF Move cable from MKRS OUT jack (J2) to DEMOD VID OUT jack (J3)	Adjust oscilloscope DIV DELAY control Until one of the pulses is centered on display. Measure pulse width at 50 percent of pulse amplitude.	Pulse width is 0.8 µsec ±0.05 µsec.	Malfunction 32
33		CHAL WIDTH SELECT switch 0.25	Measure pulse width at 50 per cent of pulse amplitude.	Pulse width is 0.25 µsec ±0.05 µsec.	Malfunction 32
34		CHAL WIDTH SELECT switch 0.50	Measure pulse width at 50 per cent of pulse amplitude	Puke width is 0.50 µsec ±0.05 µsec.	Malfunction 32

Table 3-2 Performance Test Procedure-Continued

Step No.	Oscilloscope			Performance standard	If indication is abnormal, see Table 3-3
35		CHAL WIDTH SELECT switch 1.70	Measure pulse width at 50 per cent of pulse amplitude.	Pulse width is 1.70 µsec ±0.05 µsec.	Malfunction 32
36		CHAL WIDTH SELECT switch VARY	Adjust CHAL WIDTH VARY control throughout entire range.	Pulse can be varied from less than 0.25 to more than 1.70 µsec.	Malfunction 32
		Auxiliary Modulation Delay Test			
37		CHAL WIDTH SELECT control 0.80 CHAL AUX MOD DLY control at detent position (0.2 µSEC) SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X4 SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 1.0	Adjust test set SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control until leading edge of first pulse is centered on oscilloscope graticule NOTE Do not disturb any control settings between steps 37 and 38 once pulse has been positioned.	Leading edge of pulse is centered on oscilloscope graticule.	Not applicable
38			Disconnect cable connected to test set RF IN/OUT MAIN jack and connect cable to RF IN/OUT AUX jack. Observe oscilloscope. NOTE If pulse appears but positioning is out of tolerance adjust per TM 11-6625-2611-12.	Leading edge of pulse is delayed 0.2 ±0.05 µsec from position of pulse in step 37.	Malfunction 33
39		CHAL AUX MOD DLY control fully counterclockwise SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch OFF	Repeat steps 32 thru 36.	Same as steps 32 thru 36.	Malfunction 33
40			Vary test set CHAL AUX MOD DLY control and observe position of challenge video.	Position of challenge varies with variation of CHAL AUX MOD DLY control.	Malfunction 34
		ISLS Operation Test			
41		CHAL INHIB switch ISLS ON	Observe no video.	No video is present.	Malfunction 36
42		CHAL WIDTH SELECT switch 0.80 CHAL MODE SELECT switch 2	Disconnect cable from test set RF IN/OUT AUX jack and connect to RF IN/OUT MAIN jack. Observe oscilloscope display.	Oscilloscope displays 3 pulses, P2 = 0 - +2 db above P1 and P3.	Malfunction 37

Table 3-2. Performance Test Procedure—Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal, see Table 3-3
	Oscilloscope	Test set			
43			Adjust oscilloscope DIV DELAY control until first and second pulses are displayed. Measure spacing between leading edges of first and second pulses.	Pulses are spaced 2.0 µsec ± 0.05 µ sec.	Malfunction 39
44			Using oscilloscope DIV DELAY control, center second pulse on oscilloscope display. Measure width of second pulse at 50 percent of pulse amplitude.	Pulse width is 0.8 µsec ± 0.05 µsec.	Malfunction 39
45		CHAL ISLS SPACING SELECT switch -.60	Using oscilloscope DIV DELAY control, center first and second pulses on oscilloscope display. Measure spacing between leading edges of first and second pulses.	Pulses are spaced 1.4 µsec ± 0.05 µsec.	Malfunction 39
46		CHAL ISLS SPACING SELECT switch -.15	Measure spacing between leading edges of first and second pulses.	Pulses are spaced 1.85 µsec ± 0.05 µsec.	Malfunction 39
47		CHAL ISLS SPACING SELECT switch + .15	Measure spacing between leading edges of first and second pukes.	Pulses are spaced 2.15 µsec ± 0.05 µsec.	Malfunction 39
48		CHAL ISLS SPACING SELECT switch +.60	Measure spacing between leading edges of first and second pulses.	Pulses are spaced 2.60 µsec ± 0.05 µsec.	Malfunction 39
49		CHAL ISLS SPACING SELECT switch VARY	Vary test set CHAL ISLS SPACING VARY control through its entire range. Measure spacing between first and second pulses.	Pulses spacing can be varied from less than 1.4 µsec to more than 2.60 µsec.	Malfunction 39
			Substitute Pulse Test		
50		CHAL INHIB switch OFF CHAL SUB PULSE POSITION SELECT switch -.9	Observe two pulses are present.	Two pulses are present.	Malfunction 40
51		CHAL MODE SELECT switch 3/A	Observe two pulses are present.	Two pulses are present.	Malfunction 40
52		CHAL MODE SELECT switch C	Observe two pulses are present.	Two pulses are present.	Malfunction 40
53		CHAL MODE SELECT switch 1	Observe two pulses are present	Two pulses are present.	Malfunction 40
54			Measure spacing between leading edges of pulses.	Pulses are spaced 3.9 µsec ± 0.05 µsec.	Malfunction 42

Table 3-2. Performance Test Procedure—Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal, see Table 3-3
	Oscilloscope	Test set			
55		CHAL SUB PULSE POSITION SELECT switch -.2	Measure spacing between leading edges of pulses.	Pulses are spaced 3.2 μsec ± 0.05 μsec	Malfunction 42
56		CHAL SUB PULSE POSITION SELECT switch +.2	Measure spacing between leading edges of pulses.	Pulses are spaced 2.8 μsec ± 0.05 μsec	Malfunction 42
57		CHAL SUB PULSE POSITION SELECT switch +.9	Measure spacing between leading edges of pulses.	Pulses are spaced 2.1 μsec ± 0.05 μsec	Malfunction 42
58		CHAL SUB PULSE POSITION SELECT switch VARY	Adjust test set CHAL SUB PULSE POSITION VARY control throughout entire range. Measure pulse spacing.	Pulse spacing can be varied from less than 2.0 μsec to more than 4.0 μsec	Malfunction 40
59		CHAL MODE SELECT switch 4A CHAL SUB PULSE SELECT switch M4P2 PRF SELECT X1/2.	Vary CHAL SUB PULSE POSITION VARY control. Observe pulses.	Second pulse positioning is varied.	Malfunction 40
60		CHAL SUB PULSE SELECT switch M4P3	Vary test set CHAL SUB PULSE POSITION VARY control. Observe pulses.	Third pulse positioning is varied	Malfunction 40
61		CHAL SUB PULSE SELECT switch M4P4	Vary test set CHAL SUB PULSE POSITION VARY control. Observe pulses.	Fourth pulse positioning varied.	Malfunction 40
			Mode 4 ISLS Test		
62		CHAL SUB PULSE POSITION SELECT control 0 CHAL INHIB switch ISLS ON	Adjust oscilloscope DIV DELAY control to view ISLS (fifth) pulse. Measure pulse width of fifth pulse and spacing between fourth and fifth pulses.	ISLS pulse width is 0.5 μsec ± 0.05 μsec. Pulses are spaced 2.0 μsec ± 0.07 μsec.	Malfunction 39
63			Connect oscilloscope probe between oscilloscope B INPUT and test set MODE 4 connector, pin 4. Connect oscilloscope A INPUT TO DEMOD VID OUT jack J2 Press and hold BIT (MOM) switch. Using oscilloscope DIV DELAY control locate last pulse on A INPUT. Note spacing between leading edges of pulse on A INPUT and last pulse on B INPUT. Measure width of pulse on B INPUT.	Last pulse on A INPUT and pulse on B INPUT are within ± 1.0 μsec of each other. B INPUT pulse width is 0.5 μsec ± 0.1 μsec.	Malfunction 43

Table 3-2. Perfomance Test Procedure-Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal, see Table 3-3
	Oscilloscope	Test set			
			Disparity Test		
64			Press and hold CHAL INHIB switch to DISPARITY (MOM). Note pulse in twenty sixth (66 µsec) position of A INPUT.	Pulse at twenty sixth (66 µsec) position disappears from A INPUT and appears on B INPUT.	Malfunction 43
			NOTE With various equip ments, step 65 may not he accomplished as one measurement. If test procedure cannot be accomplished as one measurement, measure spacing between fourth and last pulses on A INPUT and record spacing. Set oscilloscope MAIN TIME, DIV switch to 50 µsec and measure spacing between last pulse on A INPUT and first pulse on B INPUT and record spacing. Add results of two measurements, this should equal performance standard		
65		CHAL INHIB switch OFF PRF SELECT RANGE switch X100	Connect oscilloscope B INPUT to MODE 4 connector, pin 1. Press and hold BIT (MOM) switch.		
			Measure spacing between leading edges of fourth pulse on A INPUT and first pulse on B INPUT	Spacing between fourth pulse on A INPUT and first pulse on B INPUT is 200 µsec ± 5 µsec.	Malfunction 44
66		Press and hold BIT MOM switch. PRF SELECT RANGE XIK	Adjust oscilloscope DIV DELAY control to view three pulses on B INPUT. Measure pulse width to leading edge and spacing from leading edge.	Pulses are 0.5 ± 0.1 µsec wide and are spaced 1.8 ±0.1 µsec.	Malfunction 44
			Auxiliary Trigger Test		
67			Disconnect oscilloscope prohe between oscilloscope B INPUT and test MODE 4 connector, pin 1, Disconnect cable from oscilloscope MAIN		

Table 3-2. Performance Test Procedure-Continued

Step No.	Control settings: Oscilloscope	Control settings: Test set	Test procedures	Performance standard	If indication is abnormal, see Table 3-3
67 (Cont)			EXT INPUT and connect to EXT B INPUT. Connect cable from EXT. B INPUT to DISPLAY B INPUT. Disconnect cable from test set MEASUREMENT DEMOD VID OUT jack and connect to AUX TRIG OUT jack.		
			a. Measure width of pulse on A INPUT	a. Pulse is 1.0 ±0.5 µsec wide.	Malfunction 45
			b. Measure spacing between leading edges of pulses on A and B INPUTS.	b. Spacing between pulses is 3 ± 1.0 µsec.	Malfunction 45
		Delay Between Scope Trig and AUX Trig Test			
68		SIG GEN FCTN switch SWP ± 20 MHZ SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X0.4	Vary SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control throughout entire range.	Pulse on A INPUT can be positioned from 0.4 µsec to 4.4 µsec from pulse on B INPUT.	Malfunction 29
69		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X4 SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 10.0	Measure delay between pulse on B INPUT and pulse on A INPUT	Delay between pulses is 40 µsec ±4.0 µsec	Malfunction 29
70		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X40	Measure delay between pulse on B INPUT and pulse on A INPUT.	Delay between pulses is 400 µsec ± 40 µsec	Malfunction 29
71		SCOPE TRIG/FREQ MEAS DELAY (µEC) RANGE switch X400 SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 5.0	Measure delay between pulse on B INPUT and pulse on A INPUT	Delay between pulses is nominally 2000 µsec ± 200 µsec.	Malfunction 29
		Suppression Pulse Operation			
72		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch OFF	Remove cable from test set AUX TRIG OUT jack to oscilloscope A INPUT jack. Connect cable from test set SUPPR OU jack to oscilloscope A INPUT jack (with no termination).		
			Measure A INPUT pulse width and amplitude.	Pulse is 30 ± 3 µsec in duration, 20 ± 2 volts in amplitude.	

Table 3-2. Performance Test Procedure-Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal, see Table 3-3
	Oscilloscope	Test set			
72 (Cont)		SIG GEN FCTN switch FIXED FREQ			
			Power Output and Measurement Test		
73		MEASUREMENT FUNCTION SELECT switch PWR CHAL MODE SELECT switch 1	Reconnect test set up as shown in figure 3-22, except delete termination on oscilloscope B INPUT. Adjust MAIN TRIGGER LEVEL for stable display.		
			Adjust test set MEASUREMENT DEMOD VIDEO LEVEL control until video displayed is 1.0 volts in amplitude. Observe MEASUREMENT meter.	MEASUREMENT meter indicates 18.5 to 21.5dBW.	Malfunction 47
74			Disconnect cable from test set RF IN/OUT MAIN jack and connect to RF IN/OUT AUX jack.		
			Adjust MEASUREMENT DEMOD VIDEO LEVEL control until video is 1.0 volts in amplitude. Observe MEASUREMENT meter.	MEASUREMENT meter indicates 18.5 to 21.5dBW	Malfunction 47
			Swept Rf Test		
75		SIG GEN FCTN switch SWP ±5 MHZ	Count number of markers on B INPUT,	Seven MARKERS appear on B INPUT, are representing 0, ±1, ±3, and ±5 MHz.	Malfunction 48
		MEASUREMENT FUNCTION SELECT switch FREQ			
76			Activate and hold test set BIT (MOM) switch. Observe signal on A INPUT. Measure frequency of signal on A INPUT by interpolating between markers on B INPUT.	Frequency of signal on A INPUT is 1090 ±0.3 MHz as referenced to 1089, 1090, and 1091 MHz markers on B INPUT. For final measurement, set oscilloscope sweep display switch to DELAYED and adjust DIV DELAY control to view 1089, 1090 and 1091 MHz markers.	Malfunction 48

Table 3-2. Performance Test Procedure—Continued

Step No.	Control settings		Test procedures	Performance standard	If indication is abnormal, see Table 3-3
	Oscilloscope	Test set			
77		MEASUREMENT FUNCTION SELECT switch PRF CHAL MEASUREMENT PRF RANGE switch Xl00	Observe MEASUREMENT meter.	Meter indicates 715 to 885 pps.	Malfunction 47
78		SIG GEN FCTN switch SWP ±20 MHZ	Readjust MAIN and DELAYED TIME/DIV switches and VERNIER controls to display one complete set of markers Count markers.	Nine markers are present representing C ±1, ±3, ±5, and ±2 MHz.	Malfunction 47
79			Observe MEASUREMENT meter.	Meter indicates 220 to 280 pps.	Malfunction 47
80			Disconnect video cable and termination from oscilloscope A INPUT jack. Disconnect rf cable from test set RF IN/OUT AUX jack. Connect square law rf detector (input) directly to RF IN/OUT MAIN jack. Connect square law rf detector (output) to oscilloscope A INPUT jack using video cables.	A INPUT signal is referenced at center of oscilloscope graticule	
		CHAL MODE SELECT switch CW	Using oscilloscope A POSITION control, vertically reference A INPUT signal at center of oscilloscope graticule.		
81			Set test set MAIN ATTEN control to -11 and note amount A INPUT signal moves. (Movement equal to 1 dB change)		
82		MAIN ATTEN control -10	Measurement of signal variation between -20 MHz and +2.0 MHz markers.	Variation is less than total movement of signal in step 81 (1dB).	Malfunction 48

Table 3-3. Troubleshooting Procedure

Malfunction	Fault isolation procedures and probable causes	Corrective action
1. POWER 1.0 AMP fuseholder lights when POWER ON/OFF switch is set to ON.	a. Defective POWER l.0 AMP fuse F1 **CAUTION** If fuse faults after being replaced, isolate short in input power circuit before proceeding. Isolate using continuity check per FO-13 and FO-14.	a. Replace fuse (refer to TM 11-6625-2611-12).
	b. Defective transformer PS1T1. Isolate using continuity check per FO-14.	b. Replace transformer PS1T1 per paragraph 3-8 and 3-9.
	c. Defective connector PS1J1 or P1. Isolate using continuity check per F0-13 and FO-14.	c. Replace connector.
	d. Defective fuseholder XF1	d. Replace fuseholder XF1 per paragraph 3-8 and 3-9.
	e. Defective POWER indicator housing XDS1.	e. Replace POWER indicator housing XDS1 per paragraph 3-8 and 3-9.
2. POWER indicator does not light when POWER ON/OFF switch is set to ON.	a. Defective POWER indicator DS1	a. Replace POWER indicator lamp (Refer to TM 11-6625-2611-12).
	b. Defective POWER connector J1. Isolate using continuity check per FO-13.	b. Replace jack J1 per paragraph 3-8 and 3-9.
	c. Defective POWER ON/OFF switch S19. Isolate using continuity check per FO-13.	c. Replace switch S19 per paragraph 3-8 and 3-9.
	d. Defective POWER indicator housing XDS1.	d. Replace housing XDS1 per paragraph 3-8 and 3-9.
3. DC FAULT indicator illuminates when POWER ON/OFF switch is set to ON.	a. Using differential voltmeter, check voltage between PS1A1-TP1 (+) and GND (-). Voltage should be +27.75 to 28.25 volts. If normal proceed to step b.	a. If abnormal proceed to malfunction 4.
	b. Using differential voltmeter, check voltage between PS1A1-TP5 (+) and GND (-). Voltage should be + l2.25 to 11.75 volts. If abnormal proceed to malfunction 5. If normal, proceed to step c.	
	c. Using differential voltmeter, check voltage between PS1A1-TP6 (-) and GND (+). Voltage should be -12.25 to -11.75 volts. If abnormal proceed to malfunction 6. If normal, proceed to step d.	
	d. Using differential voltmeter, check voltage between PS1A1-TP7 (+) and GND (-). Voltage should be +4.95 to 5.05 volts. If abnormal proceed to malfunction 7. If normal, circuit card PSI is defective.	d. (1) Adjust per paragraph 3-10. (2) Replace circuit card PS1A1 per paragraph 3-8 and 3-9.
4. Improper or no voltage at PS1A1-TP1 +28 volt power supply.	a. +28 volt regulator improperly adjusted.	a. Adjust power supply per paragraph 3-10.
	b. Defective circuit card PS1A1.	b. (1) Replace circuit card PS1A1 per paragraph 3-8 and 3-9. (2) Adjust power supply per paragraph 3-10.
	c. Defective transformer PS1T1. Check secondary voltage per FO-14.	c. Check transformer PS1T1 or associated components as applicable per paragraph 3-8 and 3-9.

Table 3-3. Troubleshooting Procedure—Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
4. (Cont)	d. Defective full-wave rectifier PS1CR1/CR2 Isolate by checking diodes.	d. Replace full wave rectifier 1PS1CR1/ CR2 or associated components as applicable.
	e. Defective series regulator PS1Q1	e. Replace series regulator PS1Q1 per paragraph 3-8 and 3-9.
	f. Improper load on +28 volt power supply.	f. Check resistance between P1-A and ground with power supply unplugged. Locate actual short by disconnecting circuit cards and assemblies until short no longer exists, then replace defective assembly.
5. +12 volt power supply improper voltage, other voltages normal.	a. +12 volt regulator improperly adjusted	a. Adjust power supply per paragraph 3-10.
	b. Defective circuit card PS1A1	b. (1) Replace circuit card PS1A1 per paragraph 3-8 and 3-9. (2) Adjust power supply per paragraph 3-10.
	c. Defective transformer PS1T1. Check secondary voltage.	c. Replace transformer PS1T1 per paragraph 3-8 and 3-9.
	d. Defective full wave bridge rectifier PS1CR3-CR6. Check diodes,	d. Replace full wave bridge rectifier PS1CR3-CR6, or associated components as applicable per paragraph 3–8 and 3-9.
	e. Defective series regulator PS1Q2. Check transistor.	e. Replace series regulator PS1Q2 per paragraph 3-8 and 3-9.
	f. Improper load on +12 volt power supply.	f. Check resistance between P1-D and ground with power supply unplugged. Isolate short as previously described in paragraph 4f above.
6. -12 volt power supply improper voltage other voltages normal.	a. -12 volt regulator improperly adjusted	a Adjust power supply per paragraph 3-10.
	b. Defective circuit card PS1A1.	b (1) Replace circuit card PS1A1 per paragraph 3-8 and 3-9. (2) Adjust power supply per paragraph 3-10.
	c. Defective full wave bridge rectifier PSlCR3-CR6. Check diodes.	c. Replace full wave bridge rectifier PS1CR3-CR6, as applicable per paragraph 3-8 and 3-9.
	d. Defective series regulator PS1Q3. Check transistor.	d. Replace series regulator PS1Q3 per paragraph 3-8 and 3-9.
	e. Improper load on -12 volt power supply.	e. Check resistance between 1P1-H and ground power supply unplugged. Isolate short as previously described in 4f above.
7. +5 volt power supply improper voltage (1) Outputs is +4.75 or >+5.25 volts.	a. +5 volt regulator improperly adjusted	a. Adjust power supply per paragraph 3-10.
	b. Defective circuit card PS1A1.	b. (1) Replace circuit card PS1A1 per paragraph 3-8 and 3-9. (2) Adjust power supply per paragraph 3-10.
	c. Defective transistor PS1Q1. Check transistor.	c. Replace transistor PS1Q1 per paragraph 3-8 and 3-9.

Table 3-3. Troubelshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
7. (Cont)	d. Power supply has no load.	d. Check resistance between 1P1-J and ground with power supply disconnected and locate open circuit.
(2) Output is 0 volts.	a. Defective transformer PS1T1. Check secondary voltage.	a. Replace transformer PS1T1 per paragraph 3-8 and 3-9.
	b. Defective circuit card PS1A1.	b. (1) Replace circuit card PS1A1 per paragraph 3-8 and 3-9. (2) Adjust power supply per paragraph 3-10.
	c. Defective full wave rectifier PSlCR7/CR8. Check diodes.	c. Replace full wave rectifier PSlCR7/CR8 or associated components as applicable per paragraph 3-8 and 3-9.
	d. Defective regulator PS1Q3. Check transistor.	d. Replace regulator PS1Q3 per paragraph 3-8 and 3-9.
	e. Improper load on +5 volt power supply.	e. Check resistance between P1-J and ground with power supply unplugged. Isolate as described in 4f above.
8. POWER DC FAULT indicator does no light when pressed.	a. Defective POWER DC FAULT indicator DS1.	a. Replace DC FAULT indicator DS1 lamp. (Refer to TM 11-6625-2611-12).
	b. Defective circuit card PS1A1. Check for +28 volts at PS1A1TP1.	b. (1) Replace circuit card PS1A1 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective POWER DC FAULT indicator housing XDS1.	c. Replace DC FAULT indicator housing XDS1 per paragraph 3-8 and 3-9.
9. MEASUREMENT meter indicates no internal prf or indicated prf is out of tolerance when CHAL MODE SELECT switch is set 1, 2, 3/A, C, 4A 4B, or TEST.	Check prf count trig at TPB5 for both waveform and prf (use frequency counter to check prf). If abnormal, proceed to malfunction 10. If normal, fault is one of the following:	
	Probable Causes a. Measurement section out of adjustment.	a. Adjust per paragraph 3-10.
	b. Defective circuit card A10.	b. (1) Replace circuit card A10 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective MEASUREMENT meter Ml. Hint to check meter. Set MEASUREMENT FUNCTION SELECT switch S10 to PWR. If meter indication follows variation of MEASUREMENT DEMOD VIDEO LEVEL control, meter is probably operating.	c. (1) Replace MEASUREMENTS meter Ml per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	d. Defective MEASUREMENT FUNCTION SELECT switch S10. Isolate by continuity check per FO -12.	d. Replace MEASUREMENT FUNCTION SELECT switch S10 per paragraph 3-8 and 3-9.
	e. Defective MEASUREMENT PRF RANGE switch S9. Isolate by continuity check per FO-12.	e. Replace MEASUREMENT PRF RANGE switch S9 per paragraph 3-8 and 3-9.
10. No prf count trig at TPB5 or prf of count trig is out of tolerance.	Check 0 trig at TPA5 for both waveform and prf (use frequency counter to check prf). If abnormal, set test set SIG GEN FCTN switch to ±20 MHZ. If 0 trig is abnormal for both tests, proceed to malfunction 11. If 0 trig waveform is normal for either test or prf with SIG GEN FCTN switch set to FIXED FREQ is normal, fault is one of the following	

Table 3-3. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
10. (Cont)	*Probable causes* a. Defective circuit card A4. Check by substitution.	a. Replace circuit card per paragraph 3-8 and 3-9.
	b. Defective circuit A8.	b. (1) Replace circuit card A8 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective MEASUREMENT FUNCTION SELECT switch S10. Isolate by FO-12.	c. Replace MEASUREMENT FUNCTION SELECT switch S10 per paragraph 3-8 and 3-9.
11. No 0 trig at TPA5 or prf of 0 trig is out of tolerance	Check raw prf trig at TPA1 for both waveform and prf (use Frequency counter to check prf). If abnormal, proceed to malfunction 12. If normal, fault is onc of the following: *Probable Cause* a. Defective circuit card A3	a Replace circuit card A3 per paragraph 3-8 and 3-9.
	b. Defective CHAL MODE SELECT switch S3. Isolate by continuity check per FO-12.	b. Replace CHAL MODE SELECT switch S3 per paragraph 3-8 and 3-9.
12. No raw prf trig at TPA1 or prf of raw prf trig is out of tolerance.	a. Defective circuit card A1	a. (1) Replace circuit card Al per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defectivc PRF SELECT switch S5. Isolate by continuity check per FO-12.	b. Replace switch S5 per paragraph 3-8 and 3-9.
13. MEASUREMENTS meter indicates no internal prf or internal prf is out of tolerance when CHAL MODE SELECT switch is set to 4A or 4B, and PRF SELECT switch to X 1/2.	a. Defective circuit card A3	a. (1) Replace circuit card A3 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defect CHAL MODE SELECT switch S3, or S23 PRF SELECT switch. Isolate by continuity check per FO-12.	b. Replace switch S3 or S23 per paragraph 3-8 and 3-9.
14. Pulses missing or no challenge pulses when checking SIF modes.	a. Check 0 trig at TPA5. If abnormal, proceed to malfunction 11. If normal, one of the following:	
a. Oscilloscope is not triggered or cannot be synced. (No output at MEASUREMENT SCOPE TRIG Outback).	*Probable Causes* (1) Defective circuit card A3.	a. (1) *(a)* Replace circuit card A3 per paragraph 3-8 and 3-9. *(b)* Adjust per paragraph 3-10.
	(2) Defective SCOPE TRIG/FREQ MEAS DELAY (µSEC) switch S6. Isolate using continuity check per FO-12.	(2) Replace switch S6 per paragraph 3-8 and 3-9.
b. Only one pulse appears	b. (1) Defective circuit card A5.	b. (1) Replace card A5 per paragraph 3-8 and 3-9.
	(2) Defective CHAL MODE SELECT switch S3. Isolate using continuity check per FO-12.	(2) Replace switch S3 per paragraph 3-8 and 3-9.
15. TIMING MRKS pulses missing or out of tolerance.	a. Defective circuit card A9.	a. (1) Replace circuit card A9 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
16. No detector output at TPC5 when pressing S16 BIT (MOM)	*Probable causes* a. Defective peak PWR VID and PRF circuit card A10	a. (1) Replace circuit card A10 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective Filter/Amplifier A14	b. Replace filter/amplifier A14 per paragraph 3-8 and 3-9.

Table 3-3. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
16. (Cont)	c. Defective RF BIT/mixer assy A15.	c. Replace RF BIT/mixer assy A15 per paragraph 3-8 and 3-9.
	d. Defective rf generator assy A11.	d. Replace rf generator assy. All per paragraph 3-8 and 3-9. Adjust per paragraph 3-10.
17. No rf output on either RF IN/OUT jack	Connect oscilloscope to MAIN MOD + TPF2. If abnormal, dual modulator A16 or ISLS delay and shapers A7 defective. *Probable causes*	
	a. Defective circulator HY1	a. Replace Circulator HY1 per paragraph 3-8 and 3-9.
	b. Defective dual modulator A16.	b. (1) Replace Dual Modulator A16 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective circuit card A7.	c. (1) Replace circuit card A7 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10f and 3-l0g.
18. Rf output is out of tolerance	a. Defective rf generator All. Check by measuring rf power output at A11J3 (normally +17 dBm to +21 dBm).	a. (1) Replace rf generator All per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
19. Rf output in tolerance at both RF IN/OUT jacks, but no detector output at TPC5.	*Probable causes* *a.* Defective rf generator All. Check by measuring rf power output at A11J4. Disconnect cable W24P2 at A11J4. Connect PWR meter. (normally +7 dBm ± 2dBm)	a. (1) Replace rf generator Al1 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective cable. Using multimeter perform resistance measurements from center contact to rigid shield of applicable cables. Resistance should be greater than 10 K ohms. (FO-7). W24, W20, W1, and W22	b. Replace defective cable per FO-7.
20. No main rf but aux rf normal.	Check main mod vid at TPB4. If normal, refer to malfunction 21. If abnormal, defective circuit card A7.	a. Replace circuit card A7 per paragraph 3-8 and 3-9. b. Adjust per paragraph 3-10.
21. Main mod vid at TP B4 but no main rf output.	Check signal between mod main +(TPF2) and mod main - (TPF1). If abnormal, defective dual modulator A16. If normal, fault is one of the following: *Probable Cauaes*	a. Replace dual modulator A16 per paragraph 3-8 and 3-9. b. Adjust per paragraph 3-10.
	a. Defective dual modulator A16. Isolate by checking pulse power output at A16J2.	. (1) Redate dual modulator A16 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective coupler DC2. Isolate by checking pulse power output at DC2J1.	b. Replace coupler DC2 per paragraph 3-8 and 3-9.
	c. Defective MAIN ATTEN control AT1. Isolate by checking pulse power output at AT1J1.	c. Replace control AT1 per paragraph 3-8 and 3-9.
	d. Defective attenuator AT3.	d. Replace attenuator AT3 per paragraph 3-8 and 3-9.
	e. Defective coupler DC1.	e. Replace coupler DC1 per paragraph 3-8 and 3-9.

Table 3-3. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
22. No main mod vid signal at TPB4 or challenge pulse spacing out of tolerance (challenge generator is faulty).	Check cal work A/B gate at TPA9. If abnormal proceed to malfunction 23. If normal, circuit card A6, circuit card A7 or CHAL, WIDTH SELECT switch S4 is defective	
	Probable Causes	
	a. Defective circuit card A6. Check by measuring logic levels at TPB1 and TPB2. If either logic level is less than +3.5 volts, circuit card A6 is defective. If both logic levels are more than +3.5 volts, circuit card A6 is functioning.	a. (1) Replace circuit card A6 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-l0.
	b. Defective circuit card A7.	b. (1) Replace circuit card A7 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective CHAL WIDTH SELECT switch S4.	c Replace switch S4 per paragraph 3-8 and 3-9.
23. No chal word A/B gate at TPA9 or signal is out of tolerance,	Check counter outputs A11 and B7 at TPA7 and TPA8. If either signal is abnormal, proceed to malfunction 24. If both signals arc normal, fault is one of the following:	
	Probable Causes	
	a. Defective circuit card A5.	a. Replace circuit card A5 per paragraph 3-8 and 3-9.
	b. Defective CHAL MODE SELECT switch S3. Isolate by continuity check per FO-12.	b. Replace switch S3 per paragraph 3-8 and 3-9.
24. No counter outputs All or B7 at TPA7 and TPA8 or either signal is out o tolerance.	a. If either signal is normal, circuit card A4 is defective. If both signals are abnormal, check gated clock and counter initialize at TPA4 and TPA6, If both signals are normal, circuit card A4 is defective.	a. Replace circuit card A4 per paragraph 3-8 and 3-9.
	b. If either or both gated clock and counter initialize are abnormal, circuit card A3 is defective.	b. (1) Replace circuit card A3 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective circuit A9(clock).	(1) Replace circuit card A9 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10o.
25. Pulses at MEASUREMENT DEMOD VID OUT.	a. Defective circuit card A10	(1) Replace circuit card A10 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective MEASUREMENT FUNCTION SELECT switch S10. Isolate using continuity checks per FO-12.	b. Replace switch S10 per paragraph 3-8 and 3-9.
26. TEST mode only inoperative or signal is out of tolerance (all other modes operative)	Check test mode trig at TPB2. If signal is normal circuit card A7 is defective. If signal is abnormal, fault is one of following:	a. Replace circuit card A7 per paragraph 3-8 and 3-9. Adjust per paragraph 3-10.
	Probable causes	
	a. Circuit card A6 it out of adjustment.	Adjust per paragraph 3-10.
	b. Defective circuit card A6.	b.(1) Replace circuit card A6 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective CHAL MODE SELECT switch S3.	c. Replace switch S3 per paragraph 3-8 and 3-9.
	d. Defective, CHAL SUB PULSE SELECT switch S1.	d. Replace switch S1 per paragraph 3-8 and 3-9.

Table 3-3. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
27. Mode 4 challenge pulses missing or pulse spacing out of tolerance all other modes operating normally.	Check raw prf trig at TPA1. If abnormal, proceed to malfunction 12. If normal, fault is one of the following *Probable causes* a. Defective circuit card A5.	a. Replace circuit card A5 per paragraph 3-8 and 3-9.
	b. Defective CHAL MODE SELECT switch 3. Isolate using continuity check.	b. Replace switch S3 per paragraph 3-8 and 3-9.
	c. Defective CHAL SUB PULSE SELECT switch S1. Isolate using continuity check per FO-12.	c. Replace switch S1 per paragraph 3-8 and 3-9.
28. In DUAL 3/A no output or only one set of challenge pulses.	Check raw dly trig at TPA2. If signal is abnormal, proceed to malfunction 29. If normal fault is one of the following *Probable Causes* a. Defective circuit card A3.	a. (1) Replace circuit card A3 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective CHAL MODE SELECT switch S3. Isolate using continuity check perz FO-12.	b. Replace switch S3 per paragraph 3-8 and 3-9.
29. No raw dly trig signal at TPA2 or improper delay trigger operation	Check raw prf trig at TPA1. If abnormal, proceed to malfunction 12. If normal one of the following is defective:	
	a. Defective circuit card A2.	a. (1) Replace circuit card A2 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective SCOPE TRIG/FREQ MEAS DELAY (µSEC) switch S6.	b. Replace switch S6 per paragrapn 3-8 and 3-9.
30. No SIF reply marker output or marker positioning cannot be varied.	Check counter A11 and B7 signals at TPA4 and TPA6. If either signal is abnormal, proceed to malfunction 24. If both signals are normal, one of the following is defective:	
	a. Defective circuit card A6.	a. (1) Replace circuit card A6 per paragraph 3-8 and 3-9. b. (2) Adjust per paragraph 3-10.
	b. Defective MKR PHASING control R6. Isolate by resistance check FO-11.	b. Replace control R6 per paragraph 3-8 and 3-9.
31. SIF reply marker positioning out of tolerance.	Circuit board A6 out of adjustment.	Adjust per paragraph 3-10.
32. Challenge pulse width out of tolerance.	a. Circuit card A7 out of adjustment,	a. Adjust per paragraph 3-10.
	b. Defective circuit card A7.	b. (1) Replace circuit card A7 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	c. Defective CHAL WIDTH SELECT switch S4.	Replace switch S4 per paragraph 3-8 and 3-9.
33. No output at RF IN/OUT AUX jack or output out of tolerance.	Check output at RF IN/OUT MAIN jack. If no signal proceed to malfunction 17. If normal, fault if one of the following:	
a. Challenge pulse width out of tolerance.	a. See malfunction 32.	
b. No output	b. Check aux mod vial-signal at TPB3. If abnormal, proceed to malfunction 34. If normal, connect LOW PWR MEAS IN jack to RF IN/OUT MAIN jack and set	

Table 3-3. Troubleshooting Procedure—Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
33. (Cont)	CHAL INHIB switch to ISLS ON. It no ISIS pulse appears in challenge train refer to malfunction 35. If ISLS pulse is present fault is one of the following:	
	Probable Causes	
	a. Defective switch S21. Isolate by continuity check per FO-11.	a. Replace switch S21 per paragraph 3-8 and 3-9.
	b. Defective adhustable pad AT5. Isolate by measuring rf power at AT5J1 (should be 0±1 dBM).	b. (1) Replace adjustable pad AT5 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10*f*
	c. Defective attenator AT9.	c. Replace attenuator AT9 per paragraph 3-8 and 3-9.
	d. Defective attenuator AT4	d. Replace attenuator AT4 per paragraph 3-8 and 3-9.
	e. Defective MULT/COUPLER DC3	e. Replace DC3 per paragraph 3-9.
34. No aux mod vid signal at TPB3 or aux mod video cannot be positioned by CHAL AUX MOD DLY control	a. Defective circuit card A7	a. (1) Replace circuit card A7 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective CHAL WIDTH SELECT switch S4. Isolate by continuity check per FO-12.	b. Replace switch S4 per paragraph 3-8 and 3-9.
	c. Defective CHAL AUX MOD DLY control R6.	c. Replace control R6 per paragraph 3-8 and 3-9.
35. Improper ISLS rf output	Check signal between mod aux + and mod aux at test points TPF4 and TPF3. If abnormal, defective dual modulator A16. If normal, fault is one of the following:	a. Replace dual modulator A16 per paragraph 3-8 and 3-9. b. Adjust per paragraph 3-10.
	Probable Causes	
	a. Defective dual modulator A16. Isolate by measuring rf power at A16J4 (should be +11 ±1 dBm).	a. (1) Replace dual modulator A16 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10,
	b. Defective AUX ATTEN control ATI. Isolate by measuring rf power at ATJ1 (should be -5 ±1 dBm).	b. Replace control AT1 per paragraph 3-8 and 3-9.
	c. Defective rf switch S21	c. Replace switch S21 per paragraph 3-8 and 3-9.
36. Output occurs at RF IN/OUT AUX jack when ISLS is selected.	a. If one pulse is observed at RF IN/OUT AUX jack when CHAL INHIB switch is set to set to ISLS ON, CHAL INHIB switch S15, rf switch S20 or S21 is defective. Isolate by continuity check per FO-11.	a Replace faulty rf switch per paragraph 3-8 and 3-9.
	b. If two pulses are observed at RF IN/OUT AUX jack when CHAL INHIB switch is set to ISLS ON, CHAL INHIB switch S15 is defective.	b. Replace switch S15 per paragraph 3-8 or 3-9.
37. No ISLS pulse when ISLS is selected or pulse amplitude is out of tolerance (RF IN/OUT MAIN signal otherwise normal).	a. If ISLS pulse amplitude is out of tolerance, rf power output is improperly adjusted.	a Adjust per paragraph 3-10.
	b. If no ISLS pulse, check aux mod vid at TPB3. If abnormal proceed to malfunction 38. If normal defective rf switch S20 or rf switch S21. Isolate by continuity check FO-12.	b. Replace faulty rf switch per paragraph 3-8 and 3-9.
38. No ISLS pulse at aux mod vid test point TPB3.	a. Defective circuit card A7.	a. (1) Replace circuit card A7 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective CHAL ISLS SPACING SELECT switch S7. Isolate by continuity check per FO-12.	

Table 3-3. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
39. Improper ISLS pulse spacing or pulse width.	a. Circuit card A7 out of adjustment. b. Defective CHAL ISLS SPACING SELECT switch S7.	a. Adjust per paragraph 3-10 b. Replace switch S7 per paragraph 3-8 and 3-9.
40. Only one pulse out when substitute pulse operation is selected.	Check sub pulse trig at TPB1. If abnormal proteed to malfunction 41. If normal, circuit card A7 is defective.	a. Replace circuit card A7 per paragraph 3-8 and 3-9. b. Adjust per paragraph 3-10.
41. No sub pulse trig at TPB1	s. Defective circuit card A6.	a. (1) Replace circuit card A6 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective CHAL SUB PULSE POSITION SELECT switch S2. Isolate using continuity check per FO-12.	b. Replace switch S2 per paragraph 3-8 and 3-9.
	c. Defective CHAL SUB PULSE switch S1. Isolate using continuity check per FO-12.	c. Replace switch S1 per paragraph 3-8 and 3-9.
42. Improper substitute pulse spacing.	Circuit card A6 out of adjustment.	Adjust per paragraph 3-10.
43. Improper Mode 4 disparity operation. a. Disparity spacing is improper or pulse characteristics are out of tolerances.	a. Circuit card A8 out of tolerance.	a. Adjust per paragraph 3-10.
b. No disparity pulse output.	b. (1) Defective circuit card A8.	b. (1) (a) Replace circuit card A8 per paragraph 3-8 and 3-9. (b) Adjust per paragraph 3-10.
	(2) CHAL INHIB switch S15. Isolate using continuity checks per FO-12.	(2) Replace switch S15 per paragraph 3-8 and 3-9.
	(3) Defective BIT (MOM) switch S16. Isolate using continuity checks per FO-12.	(3) Replace switch S16 per paragraph 3-8 and 3-9.
44. No mode 4 reply output or output out of tolerance. a. Incorrect spacing or pulse width out of tolerance.	a. Circuit card A8 out of adjustment	a. Adjust per paragraph 3-10.
b. No reply output.	b. (1) Defective circuit card A8.	b. (1) (a) Replace circuit card A8 per paragraph 3-8 and 3-9. (b) Adjust per paragraph 3-10.
	(2) Defective CHAL INHIB switch S15, Isolate using continuity checks per FO-14.	(2) Replace switch S15 per paragraph 3-8 and 3-9.
45. Improper signal from AUX TRIG OUT jack.	Check counter All and B7 at TPA7 and TPA8. If either signal is abnormal, proceed to malfunction 24. If both signals are normal, fault is one of the following: a. Defective circuit card A3.	a. (1) Replace circuit card A3 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective AUX TRIG switch S14. Isolate by continuity checks per FO-14.	b. Replace switch S14 per paragraph 3-8 and 3-9.
	c. Defective AUX TRIG OUT jack J4. Isolate by continuity checks per FO-14.	c. Replace jack J4 per paragraph 3-8 and 3-9.
46. Improper signal or no signal at SUPPR OUT jack. a. Signal pulse width out of tolerance b. No signal	a. Circuit card A3 out of adjustment. b. Check 0 trig at TPA5. If abnormal, proceed to malfunction 11. If normal, fault is one of the following: (1) Defective circuit card A3.	a. Adjust per paragraph 3-10. b. (1) (a) Replace circuit card A3 per paragraph 3-8 and 3-9.

Table 3-3. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
46. (Cont)		(b) Adjust per paragraph 3-10.
	(2) Defective SUPPR switch S13. Isolate by continuity checks FO-14.	(2) Replace switch S13 per paragraph 3-8 and 3-9.
	(3) Defective SUPPR OUT jack J5. Isolate by continuity checks per FO-14	(3) Replace jack J5 per paragraph 3-8 and 3-9.
47. No indication on MEASUREMENT meter or indication is out of tolerancewhen MEASUREMENT FUNCTION SELECT switch is set to PWR.		
a. No indication regardless of DEMOD VIDEO LEVEL control setting.	a. (1) Defective MEASUREMENT meter Ml. Hint to check meter. Set MEASUREMENT FUNCTION SELECT switch to PRF CHAL. If meter indication follows variation of PRF SELECT controls meter is probably operating.	a. (1) (a) Replace MEASUREMENTS meter M1 per paragraph 3-8 and 3-9, (b) Adjust per paragraph 3-10.
	(2) Defective MEASUREMENT FUNCTION switch S10. Isolate using continuity checks per FO-12.	(2) Replace switch S10 per paragraph 3-8 and 3-9.
	(3) Defective meter adjustment board MlAl. Isolate using resistance checks per figure 3-29.	(3) (a) Replace board M1A1 per paragraph 3-8 and 3-9. (b) Adjust per paragraph 3-10.
	(4) Defective MEASUREMENT DEMOD VIDEO LEVEL control R7. Isolate by resistance check per FO-11.	(4) (a) Replace control R7 per paragraph 3-8 and 3-9. (b) Adjust per paragraph 3-10.
	(5) Defective Det/AMP (no DC level)	(5) (a) Replace Det/AMP (S/B 12 VDC level) per paragraph 3-8 and 3-9. [b) Adjust per paragraph 3-10.
b. Power indication is out of tolerance.	b. Connect power meter to RF IN/OUT MAIN jack, set test CHAL MODE SELECT switch to CW and measure rf power output, If rf power is -10 dBm ±1.0 dB, measurement section is faulty, If rf power is not -10 dBm ±1.0 dB, rf output is fault, refer to malfunction 18.	
	(1) Meter circuit out of adjustment.	3. (1) Adjust per paragraph 3-10.
	(2) Defective MEASUREMENTS meter M1.	(2) (a) Replace meter M1 per paragraph 3-8 and 3-9. (b) Adjust per paragraph 3-10.
48. Improper swept rf operation.		
a. No sweep (oscilloscope is not trig gered or cannot by synced).	a. Check sweep sync at TPE3, If abnormal proceed to malfunction 49. If normal, defective circuit card A9.	a. (1) Replace circuit card A9 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
b. Sweep occurs but no frequency markers are viewed.	b. Check rf source marker signal at XA6-39. If abnormal, proceed 10 malfunction 50. If normal, defective circuit board A6.	b. Replace circuit card A6 per paragraph 3-8 and 3-9.
c. Wrong number of markers displayed when SIG GEN switch is set to either SWP ±5 MHZ or ±20 MHZ or markers at wrong frequency.	c. Check sweep ramp signal at TPF6. If normal, defective rf generator A11 or circuit card A9 is defective.	c. Perform procedure outlined in paragraph 3-10.
d. No detected output when BIT (MOM switch is activated but markers are present.	d. Check if output at TPC5. If abnormal proceed to malfunction 51. If normal, fault is one of the following: Defective circuit card A10 or defective MEASUREMENT FUNCTION SELECT switch S10.	
	Probable causes	
	a. Defective circuit card A10.	a. (1) Replace circuit card A10 per paragraph 3-8 and 3-9.

Table 3-3. Troubleshooting Procedure-Continued

Malfunction	Fault isolation procedures and probable causes	Corrective action
48. (Cont)		*(2)* Adjust per paragraph 3-10.
	b. Defective MEASUREMENT FUNCTION SELECT switch S10. Isolate using continuity check per FO-11.	b. Replace switch S10 per paragraph 3-8 and 3-9.
	c. Defective RF BIT/Mixer	c. Replace RF BIT/mixer per paragraph *3-8* and paragraph 3-9.
e. BIT signal frequency out of tolerance (with regard to markers).	Using procedure described in table 3-17 measure frequencies of rf markers. If markers are out of tolerance, rf generator is out of adjustment. If markers are all in tolerance rf BIT/mixer A15 or if amplifier is defective.	Adjust per paragraph 3-10.
	Probable cause	
	a. RF BIT/mixer A15 is defective.	a. Replace rf BIT/mixer A15 per paragraph 3-8 and 3-9.
	b. Defective IF amplifier AR1.	b. Replace IF amplifier AR1 per paragraph 3-8 and 3-9.
49. No sweep sync at TPC3.	a. Defective circuit card A9.	a. (1) Replace circuit card per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective SIG GEN FCTN switch S17. Isolate using continuity check FO-11.	b. Replace switch S17 per paragraph 3-8 and 3-9.
50. No frequency marker signal at XA6-39.	Check sweep ramp signal at TPF6. a. If abnormal defective circuit card A6.	a. (1) Replace circuit card A6 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10
	b. If signal defective rf generator A11.	b. Perform procedure outlined in paragraph 3-9 and 3-10
51. No IF output at TPC5 or output is abnormal.	Check level of IF amp out at TPC10. If abnormal proceed to malfunction 52. If normal defective circuit card A10 or defective filter FL1.	
	Probable Causes a. Defective circuit card A10.	a. (1) Replace circuit card A10 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective filter FL1.	b. Replace filter FL1 per paragraph 3-8 and 3-9.
52. Abnormal IF amp out TPC10	a. Defective amplifier AR1.	a. Replace IF amplifier AR1 per paragraph 3-8 and 3-9.
	b. Defective rf BIT/mixer A15.	b. Replace rf BIT/mixer A15 per paragraph 3-8 and 3-9.
53. Improper meter indication when MEASUREMENT FUNCTION SELECT switch is set to PRF REPLY.	Check 50% Video width at TPC6. If abnormal defective circuit card A10. If normal fault is one of the following:	a Replace circuit card A10 per paragraph 3-8 and 3-9. b. Adjust per paragraph 3-10
	Probable causes a. Defective circuit card A8.	a (1) Replace circuit card A8 per paragraph 3-8 and 3-9. (2) Adjust per paragraph 3-10.
	b. Defective MEASUREMENT FUNCTION SELECT switch S10. Isolate by continuity check per FO-13.	b. Replace switch S10 per paragraph 3-8 and 3-9.

Section III. REMOVAL AND REPLACEMENT

3-8. Removal.

All parts may be removed using standard tools and maintenance procedures. Refer to figure 3-2 through figure 3-10 when removing parts and subassemblies.

a. Removal of Test Set Chassis, from Dust Cover

(1) Disconnect all cables from test set. (Refer to figure 3-2 for parts location.)

(2) Loosen 12 captive screws around edge of front panel (four on top, four on bottom, and two on each side).

(3) Pull test set chassis from dust cover.

b. Removal of Circuit Cards

(1) For circuit card location refer to figure 3-3.

(2) If any circuit card is to be replaced, remove circuit card retainer holding circuit cards in place. Retainer is secured by one screw at side of chassis.

c. Removal of Detector Amplifier Assy AR2

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-4 for parts location.

(2) Disconnect cable W18P2 from AR2J3 detector amplifier assy.

(3) Disconnect cable W17P2 from AR2J2 detector amplifier assy.

(4) Disconnect cable W16P2 from AR2J1 detector amplifier assy.

(5) Remove connector P6.

(6) Remove four screws securing detector amplifier to test set chassis.

d. Removal of Multicoupler Assy DC3

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-4 for parts location.

(2) Disconnect cable W18P1 from DC3J1.

(3) Disconnect cable W16P1 from DC3J2.

(4) Disconnect cable W17P1 from DC3J3.

(5) Disconnect cable W19P1 from DC3J4.

(6) Disconnect cable W15P1 from DC3J5.

(7) Disconnect cable W7P2 from DC3J6.

(8) Disconnect cable W8P2 from DC3J7.

(9) Disconnect cable W5P1 from DC3J8.

(10) Remove four screws securing multicoupler DC3 to test set chassis.

e. *Removal of R.F. Generator A11.*

(1) Remove test set chassis from dust cover, per paragraph 3-8a; refer to figure 3-4 for parts location.

(2) Disconnect cable W9P1 from rf source A11J3.

(3) Disconnect cable W24P2 from rf source A11J4.

(4) Disconnect cable W9P2 from circulator HY1J1.

(5) Slide retaining clip securing connectors P2 and P5 to rf source A11 and remove connectors.

(6) Remove four screws securing rf source A11 to test set chassis.

f. Removal of RF BIT/Mixer Assembly A15

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-5 for parts location.

(2) Disconnect cable W15P2 from rf BIT/mixer assembly A15J1.

(3) Disconnect cable W24P1 from rf BIT/mixer assembly A15J2.

(4) Disconnect cable W20P2 from rf BIT/mixer assembly A15J3.

(5) Remove two screws securing rf BIT/mixer assembly to test set chassis.

(6) Remove rf BIT/mixer assembly far enough from test set chassis to tag and identify all wired connections.

(7) Tag, identify and disconnect all wired connections between rf BIT/mixer assembly and test set chassis.

g. Removal of Dual Modulator Assembly A16

(1) Remove test set chassis from dust cover, per paragraph 3-8a; refer to figure 3-6 for parts location.

(2) Disconnect cable W25P2 from dual modulator A16J1.

(3) Disconnect cable W4P2 from dual modulator 416J4.

(4) Disconnect cable W10P1 from dual modulator A16J2.

(5) Remove four screws securing dual modulator to test set chassis.

(6) Remove dual modulator far enough from test set chassis to tag and identify all connections between dual modulator and test set chassis.

(7) Tag, identify and disconnect connections between dual modulator and test set chassis.

(8) To remove circuit board, remove four threaded standoffs securing circuit board to cavity assembly.

(9) If necessary, remove load AT6 from dual modulator A16J3.

h. Removal of Filter/Amplifier A14

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-6 for parts location.

(2) Disconnect cable W20P1 from if amplifier A14J1.

(3) Disconnect connector W22P1 from 60 MHz filter/amplifier.

(4) Remove four screws securing amplifier A14 to test set chassis.

(5) Remove if amplifier A14 far enough from test

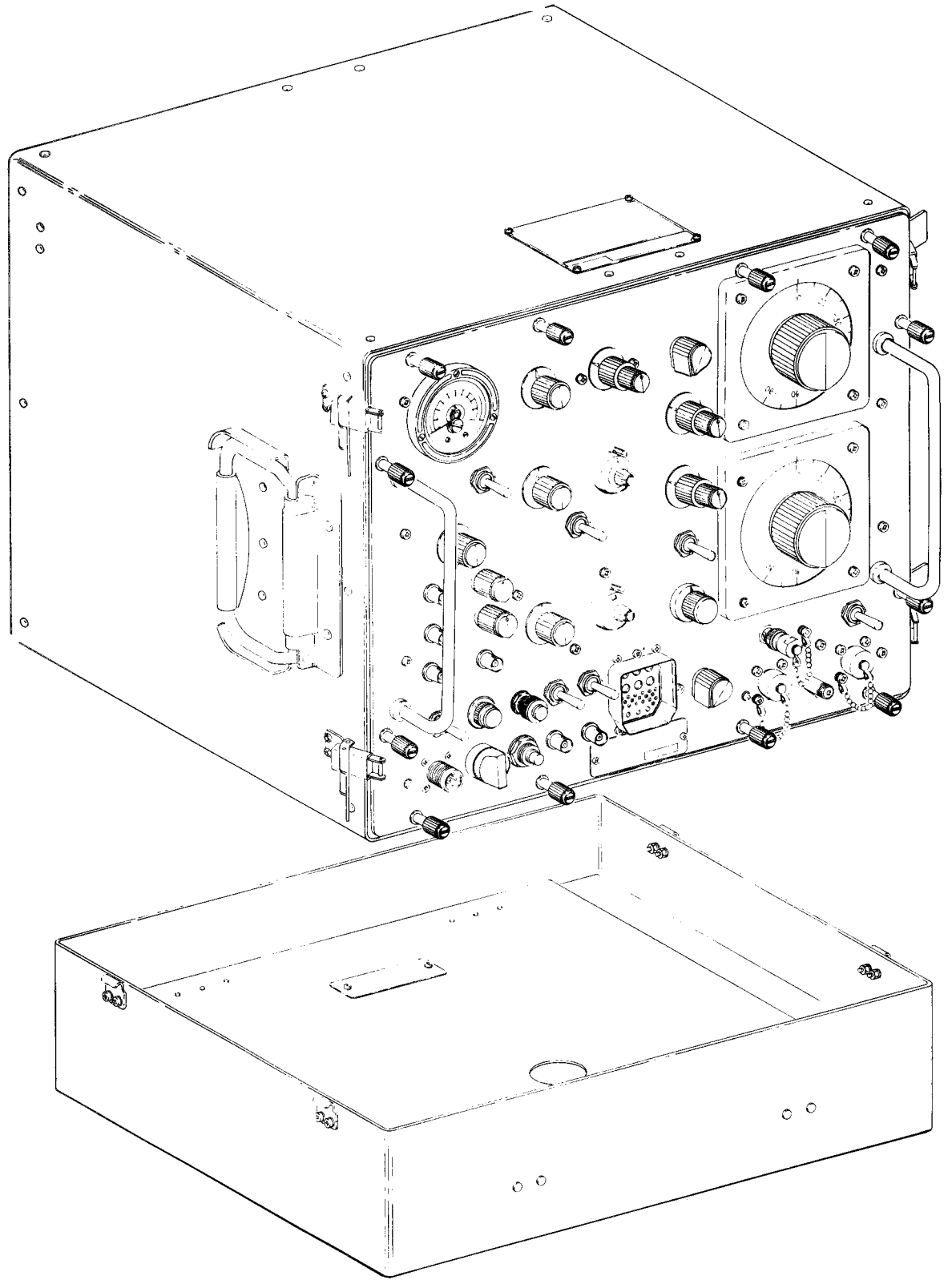


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Figure 3–2. Test set and cover assembly

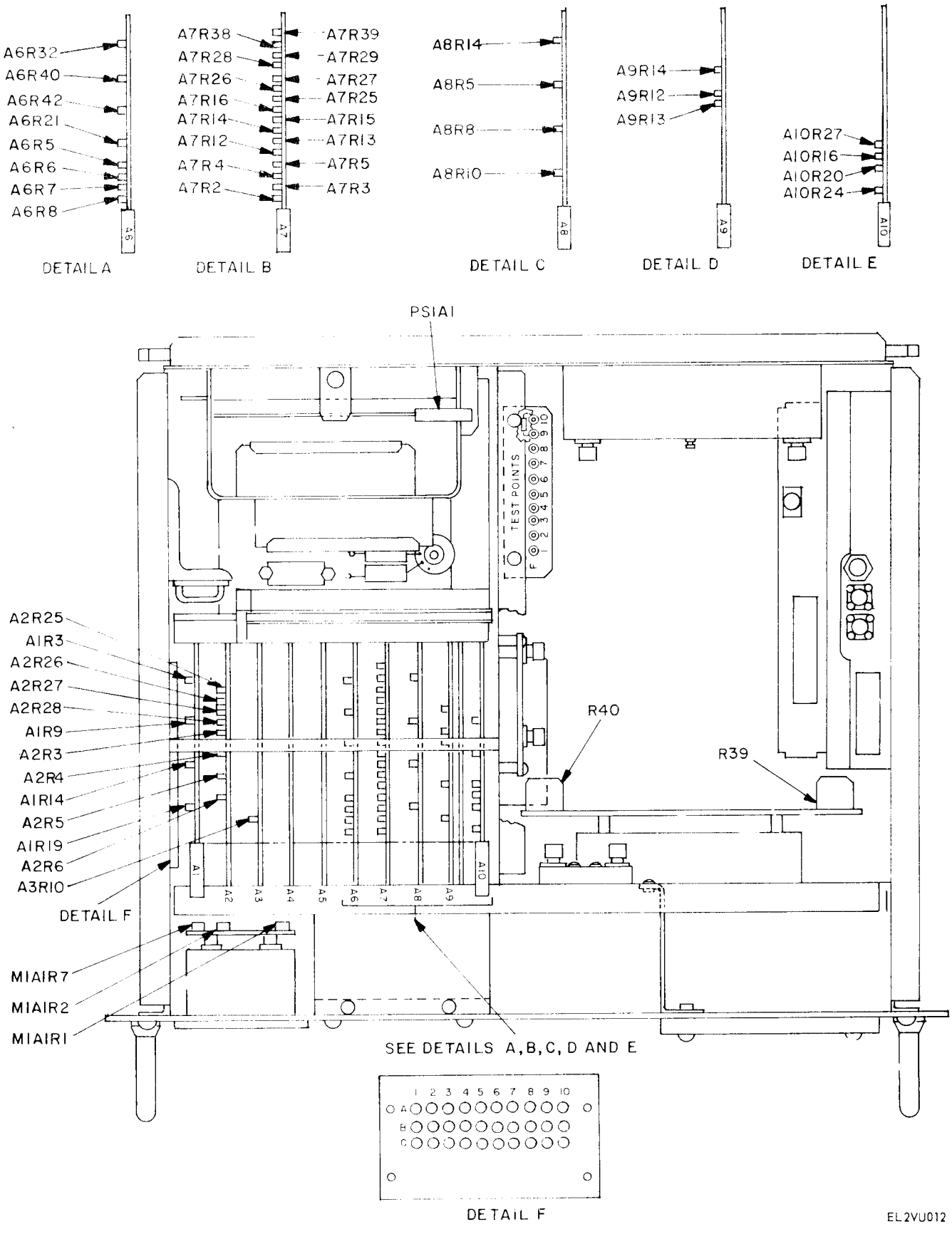

Figure 3–3. Test set location of adjustments

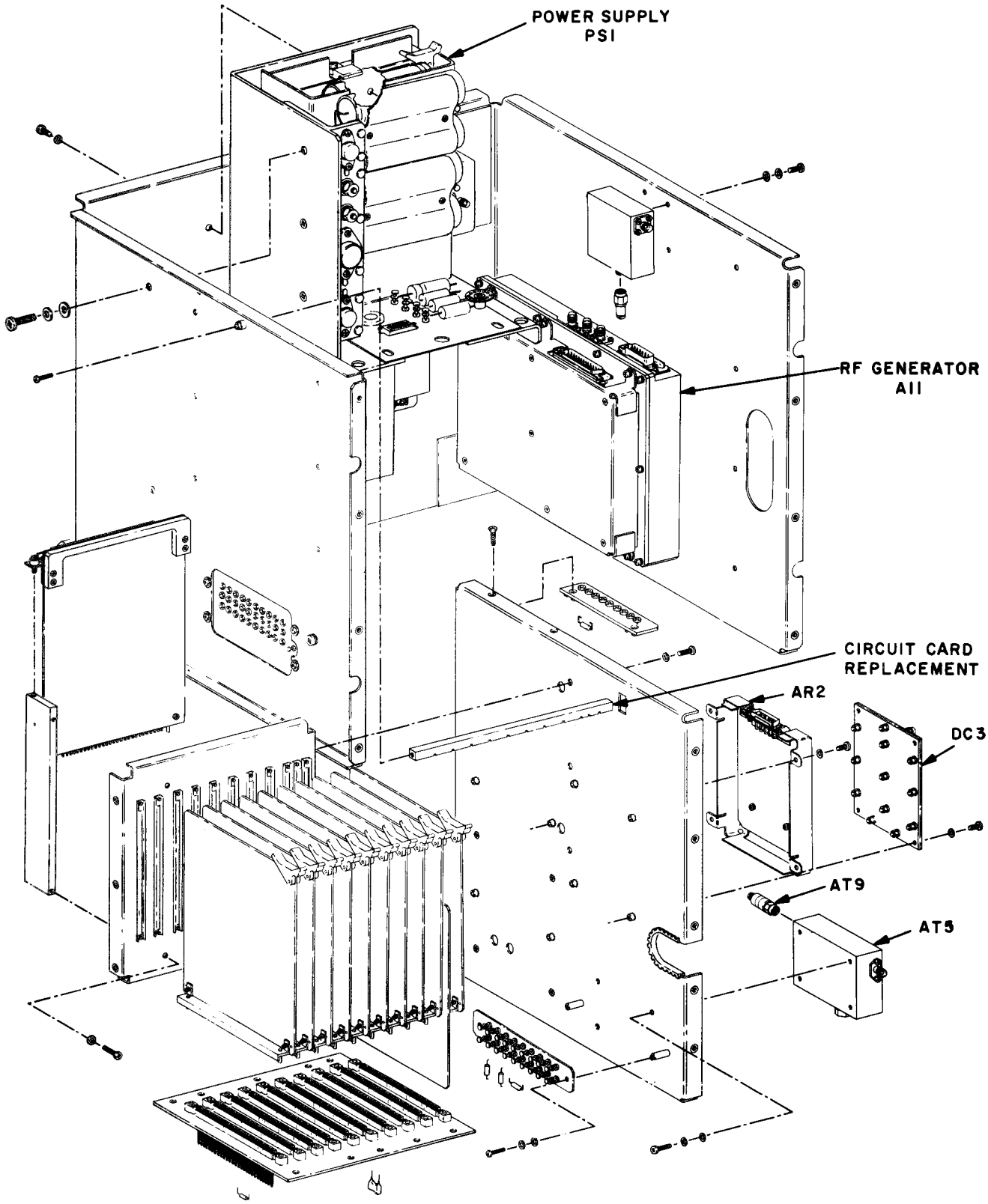

Figure 3-4. Test set power supply and card rack assembly (exploded view).

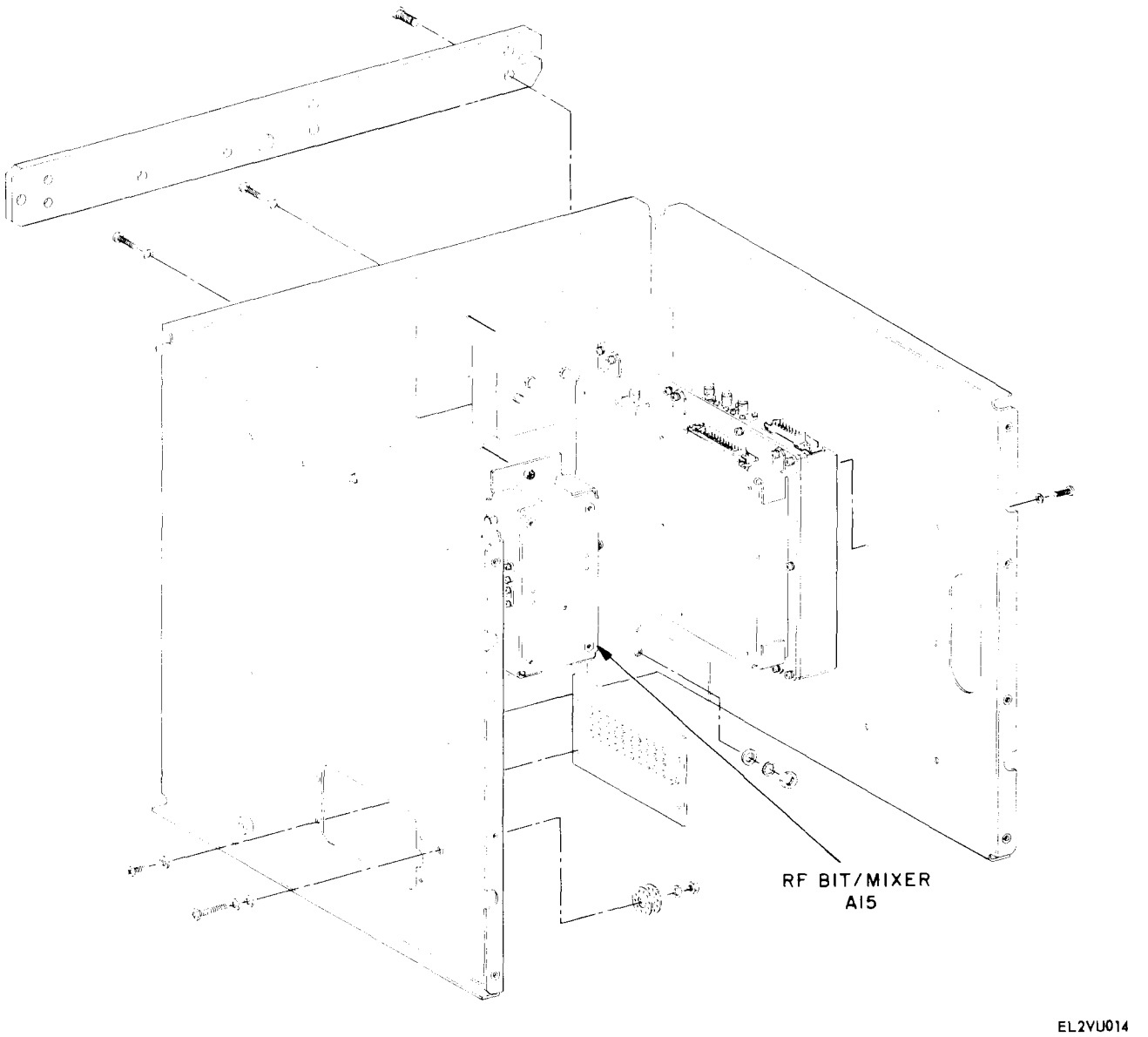

Figure 3-5. Test set RF BIT/mixer assembly (exploded view)

set chassis to tag and identify connections between if amplifier and test set chassis.

i. Control Panel Removal for Access

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-7 for parts location.

(2) Remove nut and lockwasher from LOW PWR IN jack at front of control panel.

(3) Disconnect cable W3P1 from AUX ATTEN control AT2J1.

(4) Disconnect cable W4P1 from AUX ATTEN control AT2J2.

(5) Disconnect cable W1P1 from MAIN ATTEN control AT1J1.

(6) Disconnect cable W2P1 from MAIN ATTEN control AT1J2.

(7) Remove eight screws (four on each side) from sides of control panel.

(8) Remove five screws securing control panel to brace behind MAIN and AUX ATTEN controls.

(9) Remove two screws securing front panel to brace on SCOPE TRIG/FREQ MEAS DELAY (µSEC) section of panel.

(10) Move panel away from test set chassis to clear LOW PWR IN jack and attenuators AT3 and AT4, then lay panel face down in front of test set chassis.

(11) Disassembly of individual parts is shown in figure 3-8.

j. Power Supply PS1 Removal

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-4 for parts location.

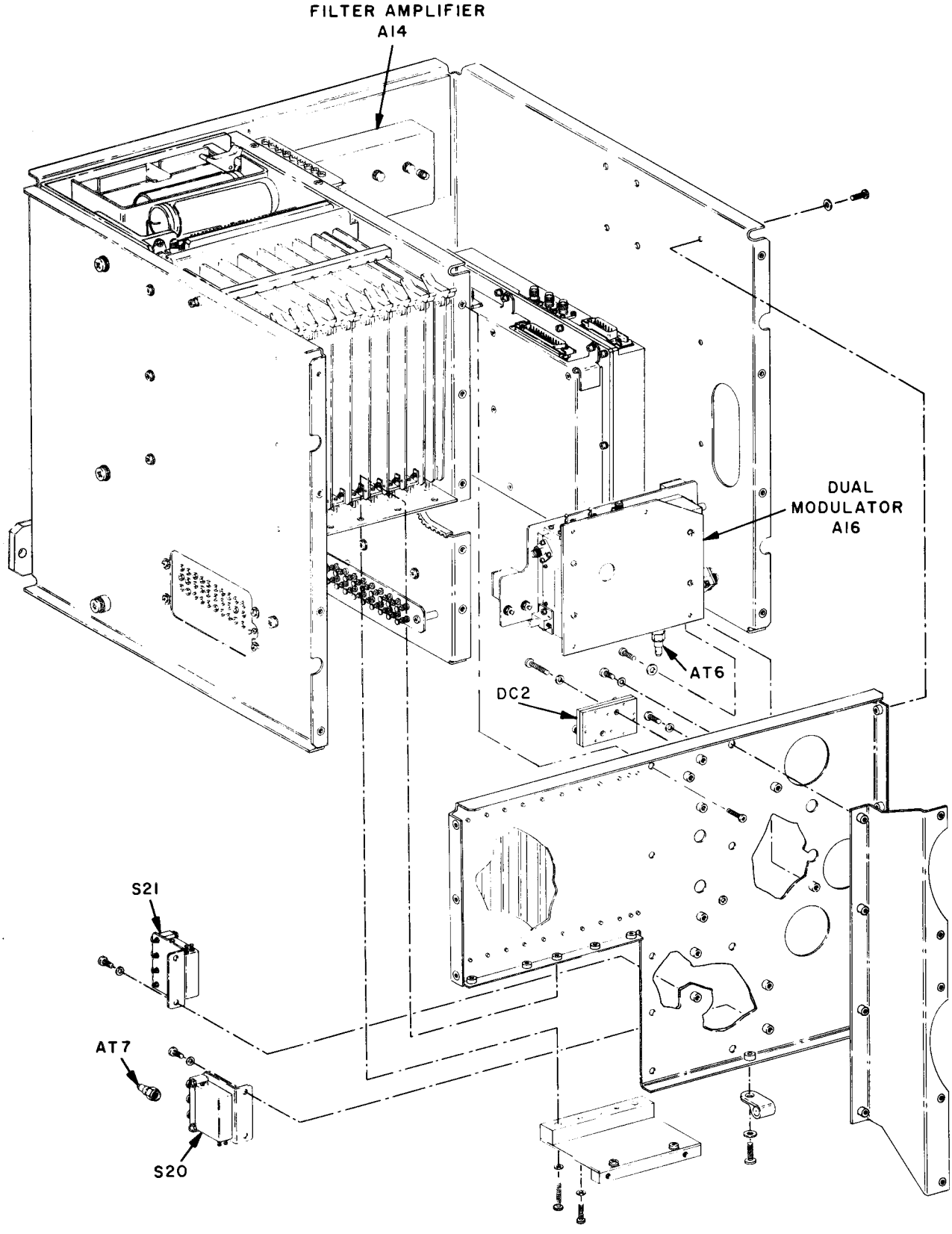

Figure 3-6. Test set chassis (exploded view).

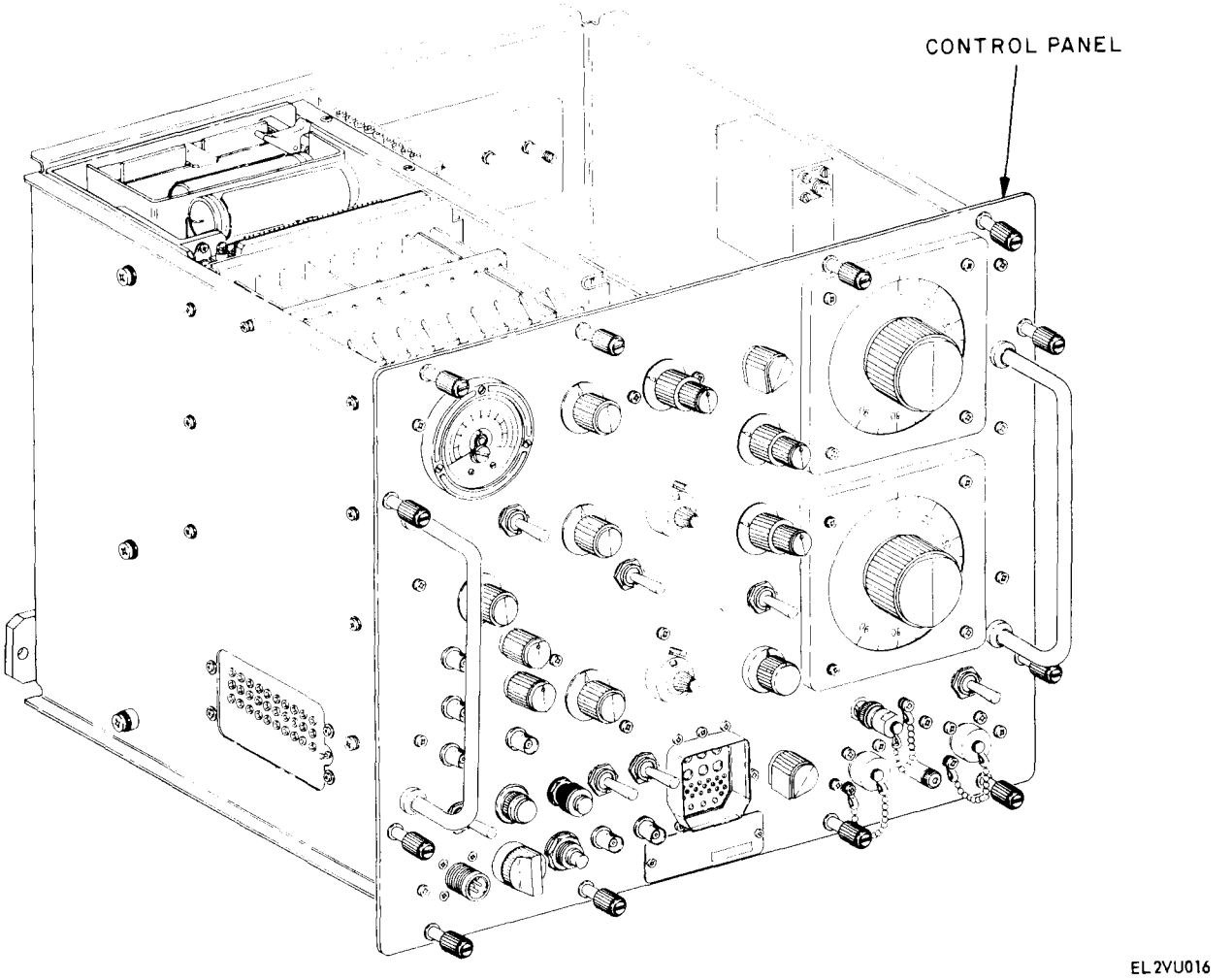

Figure 3-7. Test set control panel and circuit cards.

(2) From bottom of test set, disconnect 1P1 from power supply PS1J1.

(3) Remove seven screws securing power supply to rear of test set chassis and three screws securing power supply PS1 to side of test set chassis and two screws securing power supply to center bracket.

(4) Remove power supply PS1 from test set chassis.

(5) Remove power supply retainer by removing one screw securing retainer to bracket.

(6) Remove circuit card PS1A1 and refer to figure 3-1 for parts location.

(7) Remove six screws securing circuit card holder to power supply chassis.

(8) Remove two screws securing connector mounting bar to power supply chassis.

(9) Remove two screws securing locking bar at top of power supply.

(10) Power supply chassis should now unfold to reveal internal parts.

CAUTION

When unfolding power supply chassis use care not to damage wiring.

k. Removal of Load AT6, AT10, and AT7

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-6 for parts location.

(2) Unscrew load from connector.

l. Removal of Pad AT9

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-7 for parts location.

(2) Unscrew rf cable from pad.

(3) Unscrew pad AT9 securing pad to AT5 and remove pad from test set chassis.

m. Removal of Coupler DC1

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-5 for parts location.

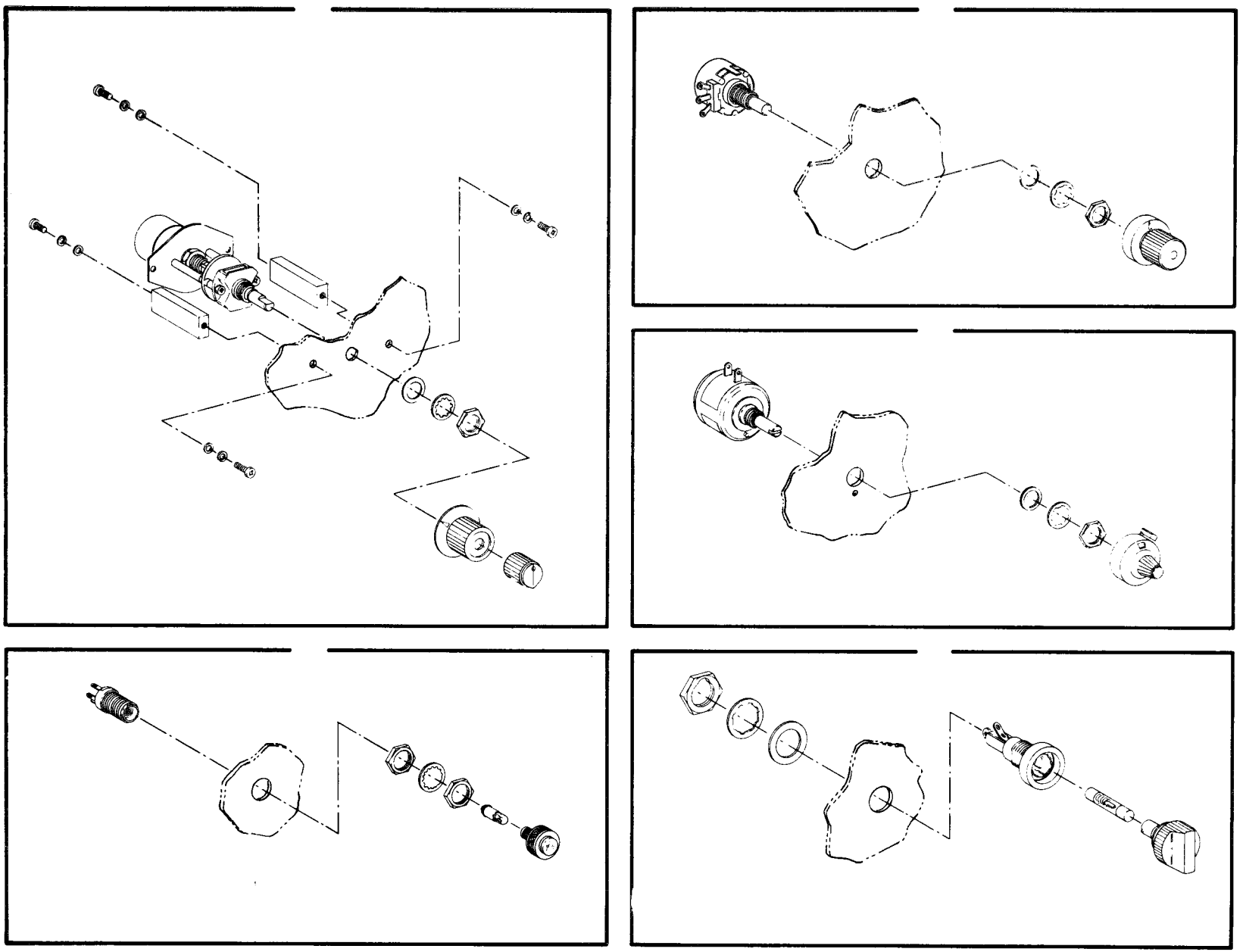

Figure 3–8. Disassembly of individual parts.

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(2) Unscrew all cables from coupler.

(3) Remove two screws securing coupler to test set front panel and remove coupler.

n. Removal of *Coupler DC2*

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-6 for parts location.

(2) Unscrew rf cables from coupler.

(3) Remove two screws securing mounting plate of coupler to test set chassis and remove coupler from chassis.

(4) Remove two screws securing mounting plate to coupler.

NOTE

Retain mounting plate and hardware for use with replacement coupler.

o. Removal of Rf Switches S20 and S21.

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-6 for parts location.

(2) Unscrew rf cabling and load (if attached) from rf switch.

(3) Remove two screws securing rf switch to test set chassis and remove switch from test set chassis.

(4) Remove soldered wires from switch and tag for future use.

p. Removal of MAIN AND AUX ATTEN Controls AT1 and AT2

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-7 for parts location.

(2) Unscrew two rf cables from control.

(3) Remove four screws, flatwashers, lockwashers, and nuts securing control to control panel and remove control from control panel.

q. Removal of Attenuators AT3 and AT4

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-9 for parts location.

(2) Unscrew rf cable from rear of attenuator.

(3) Remove four screws, lockwasher, flatwashers, and nuts securing attenuator to control panel and remove attenuator from control panel.

r. Removal of Attenuator AT5

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-4 for parts location.

(2) Disconnect cable W14P2 from AT5J1.

(3) Remove four screws and washers securing attenuator to test set chassis.

(4) Disconnect attenuator AT5 from coupler AT9 and remove attenuator from test set chassis.

s. *Removal of Circulator RF HY1*

(1) Remove test set chassis from dust cover per paragraph 3-8a; refer to figure 3-6 for parts location.

(2) Disconnect cable W9P2 from HY1J1.

(3) Disconnect cable W25P1 from HY1J2.

(4) Remove four\screws and washers securing circulator to test set chassis and remove circulator from test set chassis.

3-9. Replacement.

All parts may be replaced using standard tools and maintenance procedures. Refer to figure 3-2 through figure 3-10 when replacing parts and subassemblies.

CAUTION

Special care should be used when reinstalling semi rigid rf cabling. First start and finger tighten connections by hand, then tighten 1/16 turn further.

a. Power Supply PS1 Replacement

(1) Place power supply in test set chassis and replace three screws securing power supply to side of test set chassis; refer to figure 3-4 for part mounting location.

(2) Replace seven screws securing power supply to rear of test set chassis.

(3) Install two screws securing power supply to center bracket.

(4) Install circuit card PS1A1 in power supply chassis; refer to figure 3-1 for location.

(5) Connect connector P1 to PS1J1.

(6) Install test set chassis in dust cover per paragraph 3-9j.

CAUTION

When replacing control panel protect control panel switches and knobs from damage.

b. Control Panel Replacement

(1) Refer to figure 3-7 for individual part location and reassembly.

(2) Install control panel on front of test set chassis with LOW PWR IN jack projecting through control panel.

(3) Replace two screws which secure front panel to brace on SCOPE TRIG/FREQ MEAS DELAY (µSEC) section of panel.

(4) Replace five screws which secure brace next to MAIN and AUX ATTEN controls.

(5) Replace eight screws (four on each side which secure control panel to test set chassis).

(6) Replace nut and lockwasher on LOW PWR IN jack.

(7) Connect cable W2P1 to MAIN ATTEN control AT1J2.

(8) Connect cable W1P1 to MAIN ATTEN control AT1J1.

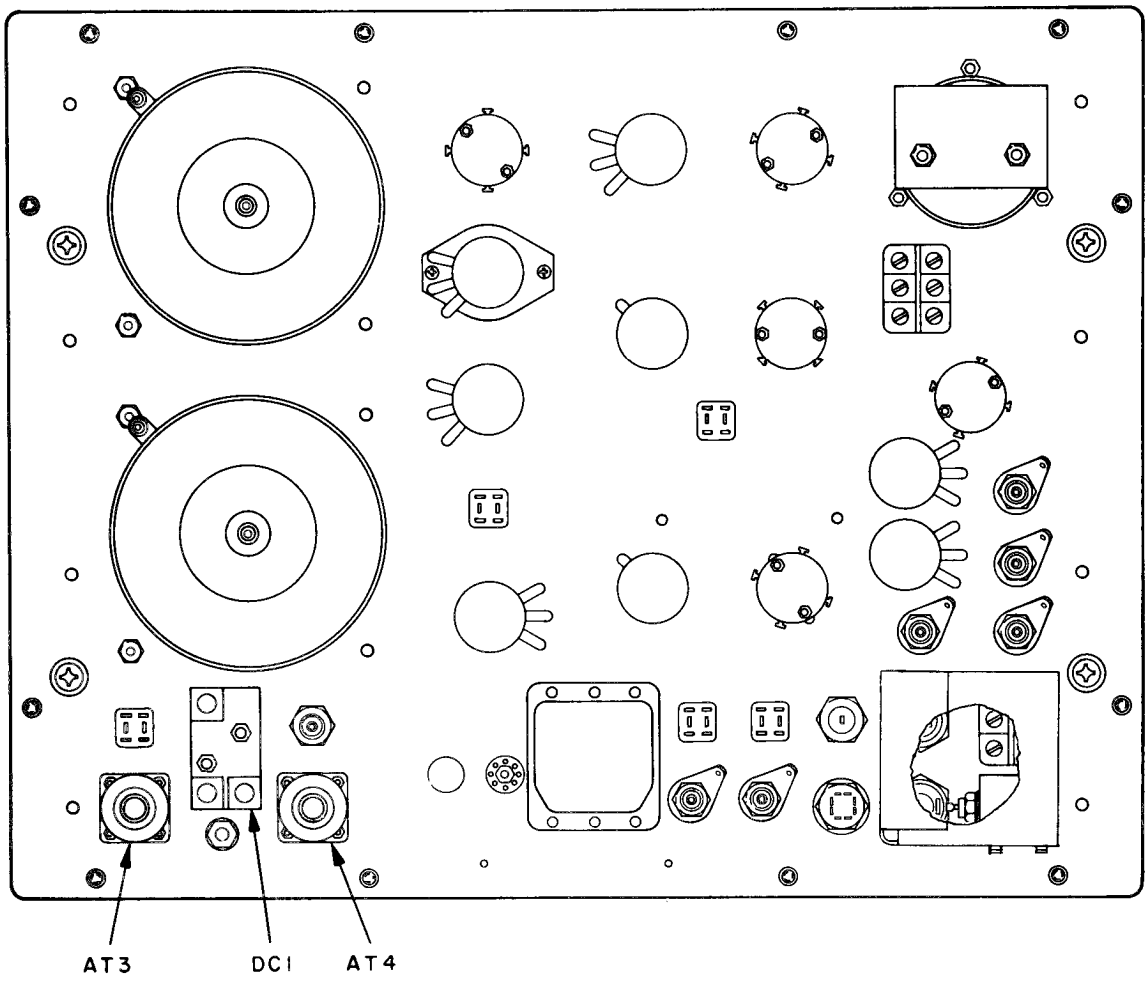


Figure 3–9. Test set control panel (rear view)

(9) Connect cable W4P1 to AUX ATTEN control AT2J2.

(10) Connect cable W3P1 to AUX ATTEN control AT2J1.

c. Filter/Amplier A14 Replacement

(1) Place Filter/Amplifier A14 on chassis. Secure with four screws and refer to figure 3-6 for parts mounting location.

(2) Connect wiring between Filter/Amplifier and test set chassis.

(3) Connect connector W22P1 to 60 MHz Filter/Amplifier.

(4) Connect cable W20P1 to if amplifier A14J1.

d. Dual Modulator A16 Replacement

(1) Place circuit board A16A1 in place on cavity assembly (figure 3-6) and secure with four threaded standoffs.

(2) If removed, replace load AT6 (figure 3-6) on dual modulator A16J3.

(3) Connect wiring between dual modulator and test set chassis.

(4) Place dual modulator A16 in place in test set chasis and secure in place with four screws.

(5) Connect cable W10P2 to dual modulator A16J2.

(6) Connect cable W4P2 to dual modulator A16J4.

(7) Connect cable W25P2 to dual modulator A16J1.

e. RF BIT Assembly A15 Replacement

(1) Connect wiring between rf BIT/mixer assembly A15 and test set chassis.

(2) Place rf BIT/mixer assembly A15 in place in test set chassis (figure 3-5) and secure with two screws.

(3) Connect cable W24P1 to rf BIT/mixer assembly A15J2.

(4) Connect cable W15P2 to rf BIT/mixer assembly A15J1.

f. Detector Amplifier Assembly AR2 Replacement

(1) Place detector amplifier assembly AR2 in place in test set chassis (figure 3-4) and secure with four screws.

(2) Connect connector P6 to detector amplifier assembly AR2.

(3) Connect cable W16P2 to AR2J1 detector amplifier.

(4) Connect cable W17P2 to AR2J2 detector amplifier.

(5) Connect cable W18P2 to AR2J3 detector amplifier.

g. Multicoupler Assy DC3 Replacement

(1) Place multicoupler assembly DC3 in place in test set chassis (figure 3-4) and secure with four screws.

(2) Connect cable W5P1 to DC3J8.

(3) Connect cable W8P2 to DC3J7.

(4) Connect cable W7P2 to DC3J6.

(5) Connect cable W15P1 to DC3J5.

(6) Connect cable W19P1 to DC3J4.

(7) Connect cable W17P1 to DC3J3.

(8) Connect cable W16P1 to DC3J2.

(9) Connect cable W18P1 to DC3J1.

h. R.F. Generator All Replacement

(1) Place rf source All in place in test set chassis (figure 3-4) and secure with four screws.

(2)) Connect connectors P2 to P5 to rf source.

(3) Connect cable W9P1 to rf source A11J3.

(4) Connect cable W24P2 to rf source A11J4.

(5) Connect cable W9F2 to circulator HY1J1.

i. Circuit *Card Replacement*

(1) Insert circuit card in correct position.

(2) If circuit card retainer is removed, replace and secure in place by one screw.

j. Test Set Chassis Installation into *Dust Cover*

(1) Slide test chassis mto dust cover. (Refer to figure 3-2 for parts location.)

(2) Tighten twelve captive screws around edge of test set front panel (four on top, four on bottom and two on each side).

k. Load AT6, AT10, and AT7 Replacement

(1) Refer to figure 3-6 for part mounting location.

CAUTION

First start and tighten load finger-tight only, then tighten 1/16 turn further

(2) Screw load onto connector.

(3) Install test set chassis in dust cover per paragraph *3-9j.*

l. Pud AT9 Replacement

(1) Refer to figure 3-4 for part mounting location.

(2) Secure pad to test set with two screws.

CAUTION

First start and tighten connections by hand. then tighten 1/16 turn further.

(3) Attach semi rigid rf cables to AT5 and DC3.

(4) Install test set chassis in dust cover per paragraph *3-9j.*

m. Coupler DC1 Replacement .

(1) Refer to figure 3-9 for part mounting location.

(2) Attach coupler to test set chassis with two screws.

CAUTION

First start and tighten connections by hand, then tighten 1/16 turn further.

(3) Attach all rf cables to coupler,

(4) Install test set chassis in dust cover per paragraph 3-9.

n. Coupler DC2 Replacement

(1) Refer to figure 3-6 for part mounting location.

(2) Attach mounting plate to coupler using two screws.

(3) Attach mounting plate to test set chassis using two screws.

CAUTION

First start and finger tighten connections by hand, then tighten 1/16 turn further.

(4) Attach rf cables to coupler.

(5) Install test set chassis in dust cover per paragraph *3-9j.*

o. RF Switches S20 and S21 Replacement

(1) Refer to figure 3-6 for part mounting location.

(2) Attach rf switch to test set chassis using two screws.

CAUTION

First start and finger tighten connection by hand, then tighten 1/16 turn further.

(3) Attach rf cabling and load (if attached) to rf switch.

(4) Install test set chassis in dust cover per paragraph *3-9j.*

p. MAIN and AUX ATTEN Controls AT1 and AT2 Replacement

(1) Refer to figure 3-10 for part mounting location.

(2) Attach control to control panel using four screws, flatwashers, lockwashers, and nuts.

CAUTION

First start and finger tighten connections by hand, then tighten 1/16 turn further.

(3) Attach rf cables to control.

(4) Install test set chassis in dust cover per paragraph 3-9j.

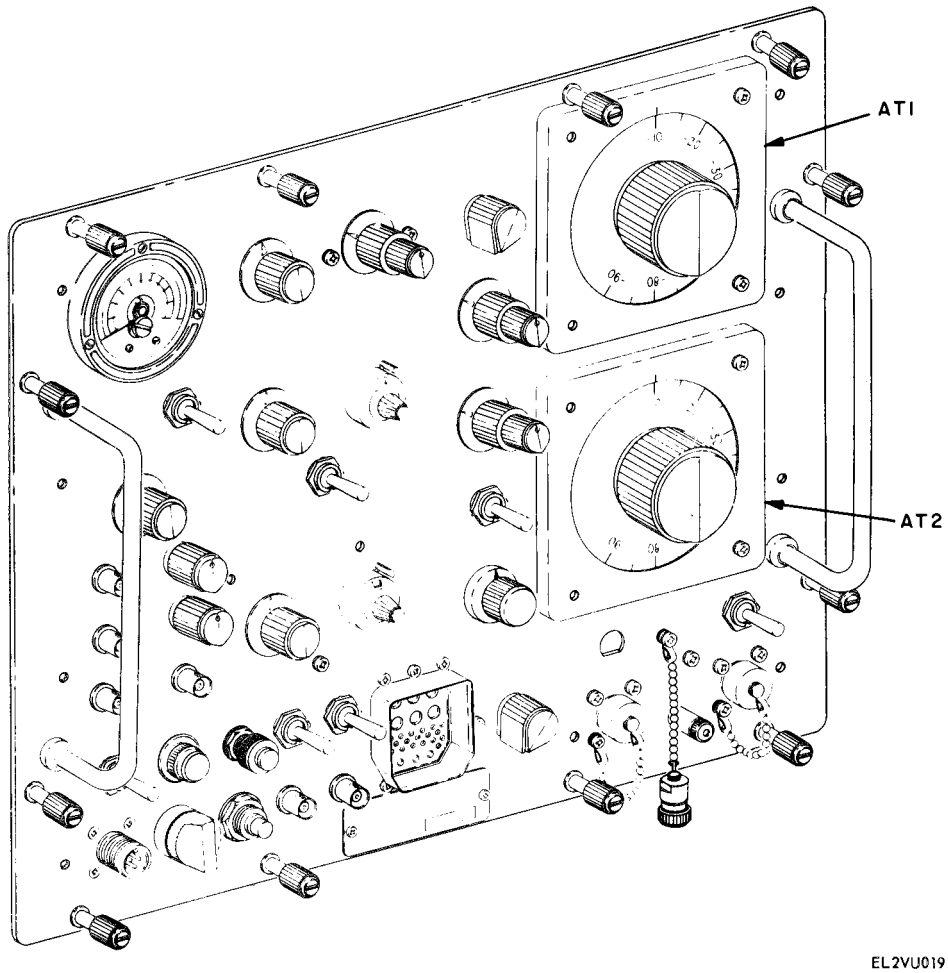


Figure 3-10. Test set control panel assembly.

q. Attenuator AT3 and AT4 Replacement

(1) Refer to figure 3-9 for part mounting location.

(2) Attach attenuator to control panel using four screws, lockwashers, flatwashers, and nuts.

CAUTION

First start and finger tighten connections by hand, then tighten 1/16 turn further.

(3) Attach rigid rf cable W6P1 to rear of attenuator AT3.

(4) Attach rigid rf cable W8P1 to rear of attenuator AT4.

(5) Install test set chassis in dust cover per pargraph *3-9j*.

r. Replacement of Attenuator AT5

(1) Place attenuator AT5 in position in test set

CAUTION

When installing rf cabling, first start and finger tighten connections by hand, then tighten 1/16 turn further.

(2) Connect attenuator AT5 to 6dB Coupler AT9.

(3) Secure attenuator AT5 to test set chassis with attenuator mounting bracket. Tighten screw securing attenuator mounting bracket to test set chassis.

(4) Connect cable W14P1 to rf switch S21.

s. Replacement of Circulator, RF HY1

(1) Place circulator HY1 in position in test set chassis, (figure 3-6) and secure with four screws and washers.

CAUTION

When installing rigid rf cabling, first start and finger tighten connections by hand, then tighten 1/16 turn further.

(2) Connect cable W25P1 to HY1J2.

(3) Connect cable W9P2 to HY1J1.

(4) If removed, replace load AT10 (figure 3-6) on circulator HY1J3.

Section IV. ADJUSTMENT AND ALIGNMENT

3-10. Adjustment Procedures.

a. Initial Procedures

(1) Use the extender board stored in the card cage as necessary for gaining access to printed circuit board test points and adjustment. On completion of procedures, remove extender board and replace printed circuit board in proper slot. Test point locations are shown in figure 3-1 and adjustment locations are shown in figure 3-3 and figure 3-11.

(2) Perform the starting procedures as outlined in paragraph 3-4.

(3) Remove power from the test set when removing or replacing circuit boards or the extender board.

b. Power Supply Adjustment

(1) Test equipment required.

(a) Transformer variable

(b) Multimeter

(c) Differential Voltmeter

(2) +28VDC circuit PS1A1.

(a) Connect test setup as shown in figure 3-13.

(b) Adjust transformer until multimeter indicates 115 vat.

(c) Locate power supply regulator board PS1A1, figure 3-3.

(d) Set differential voltmeter NULL switch to VTVM.

(e) Connect differential voltmeter (+) probe to PS1A1TP1 and (-) probe to GND. (Figure 3-11)

(f) Locate power supply adjustment pots of PS1A1, figure 3-11.

NOTES

(1) Operate differential voltmeter in accordance with procedures in TM 11-6625-537-15.

(2) Test set must be complete and operating to perform following steps.

(g) Adjust PS1A1R4 until differential voltmeter indicates +28.0 volts.

(h) Remove (+) differential voltmeter probe from PS1A1TP1.

(3) +28vdc fault circuit PS1A1.

(a) Connect (+) differential voltmeter probe to PS1A1TP8.

(b) Adjust PS1A1R18 until differential voltmeter indicates 0.00 volts.

(c) Connect (+) differential voltmeter probe to PS1A1TP1.

(d) Adjust PS1A1R4 until differential voltmeter indicates +28.20 volts.

(e) D.C. F.AULT indicator on test set should be extinguished.

(f) Adjust PS1A1R4 until differential voltmeter indicates +29.10 volts.

(g) D.C. FAULT indicator on test set should be illuminated.

(h) Adjust PS1A1R4 until differential voltmeter indicates +27.80 volts.

(i) D.C. FAULT indicator on test set should be extinguished.

(j) Adjust PS1A1R4 until differential voltmeter indicates +26.90 volts.

(k) D.C. FAULT indicator on test set should be illuminated.

(l) Adjust PS1A1R4 until differential voltmeter indicates +28.00 volts

(m) Remove differential voltmeter probes.

(4) +12 vdc circuit PS1A1.

(a) Connect differential voltmeter (+) probe to PS1A1TP5 and (-) probe to GND.

(b) Adjust PS1A1R26 until differential voltmeter indicates +12.00 volts.

(c) Remove (+) differential probe from PS1A1TP5.

(5) -12 vdc circuit PS1A1.

(a) Connect (-) differential voltmeter probe to PS1A1TP6 and (+) probe to GND.

(b) Adjust PS1A1R32 until differential voltmeter indicates -12.00 volts.

(c) Remove Differential voltmeter probes.

(6) +5 vdc circuit PS1A1

(a) Connect (+) differential voltmeter probe to PS1A1TP7 and (-) probe to GND.

(b) Adjust PS1A1R36 until differential voltmeter indicates +5.00 volts.

(7) +12 vdc fault circuit PS1A1.

(a) Connect (+) differential voltmeter probe to PS1A1TP2.

(b) Adjust PS1A1R8 until differential voltmeter indicates 300 mv.

(c) Connect (+) differential voltmeter probe to PS1A1TP5.

(d) Adjust PS1A1R26 until differential voltmeter indicates +12.20 volts.

(e) D.C. FAULT indicator on test set should be extinguished.

(f) Adjust PS1A1R26 until differential voltmeter indicates +13.10 volts.

(g) D.C. FAULT indicator on test set should be illuminated.

(h) Adjust PS1A1R26 until differential voltmeter indicates +11.80 volts.

(i) D.C. FAULT indicator on test set should be extinguished.

(j) Adjust PS1A1R26 until differential voltmeter indicates +10.90 volts.

(k) D.C. FAULT indicator on test set should be illuminated.

(1) Adjust PS1A1R26 until differential voltmeter indicates +12.00 volts.

(m) Remove differential voltmeter probes.

(8) -12 vdc fault circuit PS1A1.

(a) Connect (-) differential voltmeter probe to PS1A1TP9 and (+) probe to GND.

(b) Adjust PS1A1R23 until differential voltmeter indicates -300 mv.

(c) Connect (-) differential voltmeter probe to PS1A1TP6.

(d) Adjust PS1A1R32 until differential voltmeter indicates -12.20 volts.

(e) D.C. FAULT indicator on test set should be extinguished.

(f) Adjust PS1A1R32 until differential voltmeter indicates -13.10 volts.

(g) D.C. FAULT indicator on test set should be illuminated.

(h) Adjust PS1A1R32 until differential voltmeter indicates -11.80 volts.

(i) D.C. FAULT indicator on test set should be extinguished.

(j) Adjust PS1A1R32 until differential voltmeter indicates -10.9 volts.

(k) D.C. FAULT indicator on test set should be illuminated.

(l) Adjust PS1A1R32 until dvm indicates -12.00 volts.

(m) D.C. FAULT indicator on test set should be extinguished.

(9) +5 vdc fault circuit PS1A1.

(a) With (+) differential voltmeter probe connected to PS1A1TP7 and (-) probe to GND. Adjust PS1A1R36 until differential voltmeter indicates +5.20 volts.

(b) D.C. FAULT indicator on test set should be extinguished.

(c) Adjust PS1A1R36 until differential voltmeter indicates +4.80 volts.

(d) D.C. FAULT indicator on test set should be extinguished.

(e) Adjust PS1A1R36 until differential voltmeter indicates +5.0 volts.

(f) Remove differential voltmeter probes.

c. Internal PRF Adjustments

(1) Test equipment required–Frequency Counter

(2) Connect test setup as shown in figure 3-14.

(3) Locate prf generator board A1, figure 3-3.

(4) Set test set controls per table 3-1 except set PRF SELECT MULT control to 1.0.

(5) Set frequency counter controls for 1.00 KC.

(6) Adjust A1R9 until frequency counter indicates 1 ± 0.1 KC.

(7) Set test set PRF SELECT MULT control to 10.0.

(8) Adjust A1R3 until frequency counter indicates 10 ± 1 KC.

(9) Set test set PRF SELECT RANGE switch to X100 and PRF SELECT MULT control to 1.0.

(10) Adjust A1R14 until frequency counter indicates 0.1 ± 0.01 KC.

(11) Set test set PRF SELECT RANGE switch to Xlo.

(12) Adjust A1R19 frequency counter indicates 0.010 ± 0.001 KC.

d. Output Trigger Adjustments

(1) Test equipment required-Oscilloscope.

(2) Adjust procedure.

(a) Connect test setup as shown in figure 3-15, except for AUX TRIG OUT cable.

(b) Set test controls per table 3-1 except for PRF SELECT RANGE switch to X100 and SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch to X0.4 and set MULT to 2.50.

NOTE

If adjustment in step *(c)* (See figure 3-3 for A2 Board Adjustments) cannot be made, perform steps *(d)* and *(e)*, then return to step *(c)*.

(c) Adjust A2R28 until delay from leading edge of A INPUT pulse to falling edge of B INPUT pulse is 1.0 µsec.

NOTE

All subsequent delay measurements between the oscilloscope A and B INPUTS are from the same points as described in step (c).

(d) Set test set SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control to 11.0.

(e) Adjust test set potentiometer A2R6 until delay between pulses on B and A INPUTS is 4.4 µsec.

NOTE

Repeat steps *(c)* thru *(e)* until no further improvement is noted.

(f) Set test set SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch to X4.

NOTE

If adjustment in step *(g)* cannot be made perform steps *(h)* and *(i)*, then return to step *(g)*.

(g) Adjust test set potentiometer A2R5 until delay between pules on oscilloscope B and A INPUTS is 44 µsec.

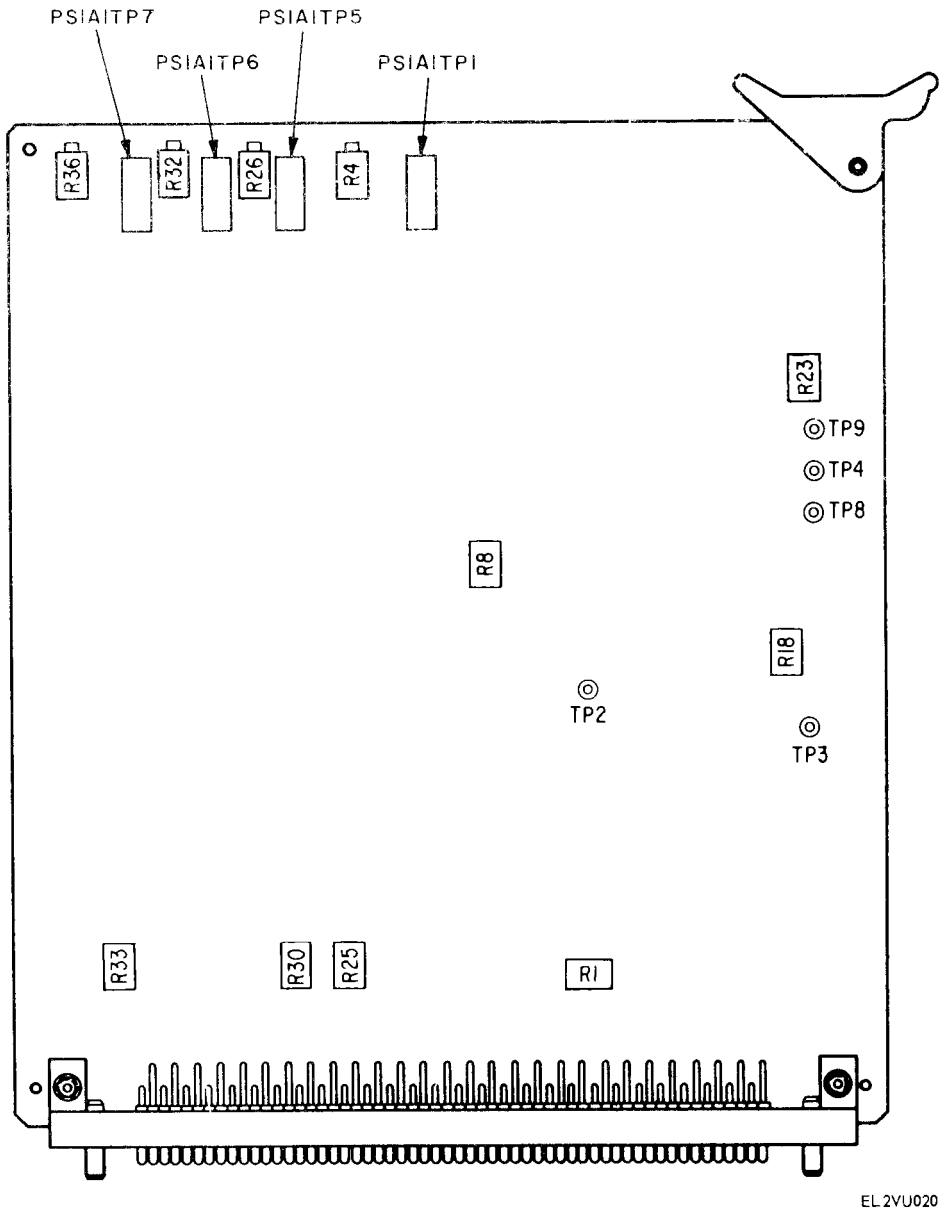


Figure 3-11. Adjustments of power supply PS141

(h) Set test set SCOPE TRIG/FREQ MEAS DELAY (uSEC) MULT control to 1.00.

(i) Adjust test set potentiometer A2R27 until delay between pulses on oscilloscope B and A INPUTS is 4 µsec.

NOTE

Repeat steps *(g)* thru (i) until no further improvement is noted.

(j) Set test set SCOPE TRIG/FREQ MEA S DELAY µSEC) RANGE switch to X40 and MULT control to 11.0.

NOTE

If adjustment in step *(k)* cannot be made perform steps *(l)* and *(m),* then return to step *(k).*

(k) Adjust test set potentiometer A2R4 until delay between pulses on oscilloscope B and A INPUTS is 440 µsec.

(l) Set SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control to 1.0.

(m) Adjust test set potentiometer A2R26 until delay between pulses is 40 µsec.

NOTE

Repeat steps *(j)* thru *(w)* until no further improvement is noted.

(n) Set test set SCOPE TRIG/FREQ MEAS DELAY µSEC) RANGE switch to X400.

NOTE

If adjustment in step *(a)* cannot be made, perform steps *(p)* and *(q)*, then return to step *(a)*.

(o) Adjust test set potentiometer A2R25 until delay between pulses is 400 µsec.

(p) Set test set SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control to 11.0.

(q) Adjust test set potentiometer A2R3 until delay between pulses is 4400 µsec.

NOTE

Repeat steps *(n)* thru *(q)* until no improvement is noted.

(r) Set test set SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch to OFF.

e. Challenge Code Substitute Pulse Adjustments

(1) Test equipment required-Oscilloscope

(2) Adjustment procedure

(a) Connect test setup as shown in figure 3-18, connect video cable to oscilloscope Main EXT INPUT and SCOPE TRIG OUT of test set.

(b) Set test set PRF SELECT RANGE switch to X1K, CHAL MODE SELECT switch to 1, and CHAL SUB PULSE POSITION SELECT switch to -.9. Connect video cable to DEMOD VID OUT and B channel of oscilloscope through a 75 ohm load.

(c) Observe that two pulses are displayed on oscilloscope; adjust test set potentiometer A6R5 until pulses are spaced 3.9 µsec. from leading edge to leading edge.

(d) Adjust oscilloscope to display only the 1st pulse.

(e) Adjust The DIV DELAY control ccw until the 2nd pulse on the A INPUT is displayed; count the number of marker cycles from the intersection point on the 1st pulse (step *f)* to same point on the leading edge of the 2nd A INPUT pulse.

(f) Adjust A6R5 until the markers indicates a pulse spacing of 3.9 ± 0.05 µsec.

(g) Set test set CHAL SUB PULSE POSITION SELECT switch to -.2.

(h) Repeat step *(c)*, but adjust test set potentiometer A6R6 for a pulse spacing of 3.2 µsec.

(i) Repeat step *(d)*.

(j) Adjust A6R6 until the markers indicate a pulse spacing of 3.2 ± 0.5 µsec.

(k) Set test set CHAL SUB PULSE POSITION SELECT switch to +.2.

(l) Repeat step *(c)* but adjust test set potentiometer A6R7 for a pulse spacing of 2.8 µsec.

(m) Repeat step *(d)*.

(n) Adjust A6R7 until the markers indicate a pulse spacing of 2.8 ± 0.5 µsee.

(o) Set test CHAL SUB PULSE POSITION SELECT switch to +.9.

(p) Repeat step *(c)* but adjust test set potentiometer A6R8 for a pulse spacing of 2.1 µsec.

(q) Repeat step *(d)*.

(r) Adjust A6R8 until the markers indicate a pulse spacing of 2.1 ± 0.5 µsec.

f. Challenge Code Pulse and RF Power Output Adjustment

(1) Test equipment required.

(a) Oscilloscope.

(b) Square law detector.

(c) Pulse power calibrator set.

(d) RF power test set.

(2) Adjustment procedures.

(a) Connect test setup as shown in figure 3-17.

(b) Set test set controls per table 3-1 except set PRF SELECT MULT control to 10.0.

(c) Measure pulse rise and fall times as 1% and 81% amplitude points. Pulse rise time should be 0.05 to 0.1 µsec and pulse fall time should be 0.05 to 0.20 µsec.

NOTE

Adjustment of A16A1R40 for ideal rise and fall times can result in excessive pulse insertion loss. Perform step *(d)* only if pulse rise and fall times are not within limits given in step *(c)*. If pulse rise and fall times are within limits given, proceed to step (e).

(d) Adjust A16A1R40 until pulse rise time is 0.05 to 0.1 µsec and pulse fall time is 0.05 to 0.20 µsec.

(e) Set test CHAL MODE SELECT switch to CW and perform procedure described in table 3-16, steps 7 and 9. If cw to pulse power difference is out of tolerance, reconnect W6P1 to AT3J1, reconnect test setup as shown in Figure 3-17 and repeat steps *(d)* and *(e)* adjusting A16A1R40 until criteria for both rise and fall times and cw to pulse power difference is met.

(f) Reconnect W6P1 to AT3J1 and W8P1 to AT4J1 if disconnected.

(g) Perform procedure described in table 3-16, step 1 while adjusting A11A2R26 until power output is -10 dBm.

(h) Connect test setup as shown in figure 3-17, except connect square law detector to test set RF IN/OUT AUX jack.

(i) Measure pulse rise and fall times at 1% and 81% amplitude points. Pulse rise time should be 0.05 to 0.1 µsec and pulse fall time should 0.05 to 0.20 µsec.

NOTE

Adjustment of A16A1R39 for ideal pulse rise and fall times can result in excessive pulse insertion loss. Perform step *(j)* only if pulse rise and fall times are not within limits given in step *(i)*. If pulse rise and fall times are within limits given, proceed to step *(k)*.

(j) Adjust A16A1R39 until pulse rise time is 0.05 to 0.1 and pulsce fall time is 0.05 to 0.20 µsec.

(k) Perform procedure described in table 3-16, steps 8, 10, and 11. If cw to pulse power difference is out of tolerance, reconnect W8P1 to AT4J1, reconnect test setup as shown in figure 3-17 and repeat steps *(i)* and *(j)* adjusting A16A1R39 until criteria for both rise and fall times and cw to pulse difference is met.

(l) Reconnect W8P1 to AT4J1 if disconnected.

(m) Connect test setup as shown in figure 3-17, except for 10X probe and rf cable, set test set controls as described in step *(b)* except set CHAL INHIB switch to ISLS ON.

(n) Set oscilloscope INT.

(o) Adjust test set AUX ATTEN control until amplitudes of P1 and P2 pulses are equal.

(p) Loosen two set screws which secure AUX ATTEN control knob and without disturbing control setting, remove knob.

(q) Loosen two screws revealed by removal of AUX ATTEN control knob and without disturbing control shaft setting position dial to indicate -10 dBm.

(r) Tighten screws and replace knob.

(s) Set test set CHAL INHIB switch to OFF and CHAL MODE SELECT switch to CW.

(t) perform table 3-16, step 4 and adjust AT5 until power output is -10dBm.

(u) Loosen locking screw on ISLS scale of AT2 and set reference to zero.

(v) perform procedure described in table 3-9, steps 22 through 28 while adjusting as listed below until pulse widths are in tolerance:

Table 3-9 Step	*Adjustment*
22	None
23	A7R15
24	None
25	None
26	A7R13
27	A7R14
28	A7R16

(w) Set test set CHAL WIDTH SELECT switch to VARY.

(x) Using 0.1 µsec. markers, adjust the test set CHAL WIDTH VARY control for a pulse width of 0.08 µsec at 50% of pulse amplitude.

(y) Disconnect input of square law detector from test set RF IN/OUT MAIN jack, and connect to RF IN/OUT AUX jack.

(z) Using 0.1 µsec markers, adjust A7R38 until pulse width is equal to pulse width set in step *(x)*.

(aa) Set test set CHAL WIDTH SELECT switch to 0.80. Reperform table 3-9 steps 23 through 28 for auxiliary output while adjusting as listed below until pulse widths are in tolerance:

Table 3-9 Step	*Adjustment*
23	A7R8
24	None
25	None
26	A7R6
27	A7R7
28	A7R9

g. ISLS Pulse Adjustments

(1) Test equipment required-Oscilloscope.

(2) Adjustment procedure.

NOTE

The following procedure references steps in table 3-10, ISLS Function Test Procedure.

(a) Perform step 1, and adjust test set potentiometer A7R27 until pulse spacing is 2 ± 0.05 µsec.

(b) Perform step 2, and adjust test set potentiometer A7R39 until pulse width is 0.8 ± 0.05 µsec.

(c) Perform step 3, and adjust test set potentiometer A7R38 until pulse width is 0.5 ± 0.05 µsec.

(d) Set oscilloscope sweep display switch to MAIN, and DELAYED TIME/DIV switch to OFF.

(e) Perform step 6, and adjust test set potentiometer A7R25 until pulse spacing is 1.40 ± 0.05 µsec.

(j) perform step 7, and adjust test set potentiometer A7R26 until pulse spacing is 1.85 ± 0.05 µsec.

(g) Perform step 8, and adjust test set potentiometer A7R28 until pulse spacing is 2.15 ± 0.05 µsec.

(h) Perform step 9, and adjust test set potentiometer A7R29 until pulse spacing is 2.60 ± 0.05 µsec.

h. Suppressor *Pu1se Adjustments*

(1) Test equipment required-Oscilloscope

(2) Adjustment procedure

(a) Perform steps 1 and 2 of table 3-11, Suppressor Pulse Function Test Procedure.

(b) Adjust A3R10 until pulse width is 30 ± 3 µsec at 50% of pulse amplitude.

i. Mode 4 Reply Output Adjustment

(1) Test equipment required,

(a) Oscilloscope

(b) Pulse Generator

(2) Adjustment procedure.

NOTE

The following procedure references steps in table 3-12, Mode 4 Interface Input and Output Function Test Procedure.

(a) Peform step 1, and adjust test set potentiometer A8R5 until pulse spacing is 200 ± 5 µsec.

(b) Perform step 2, and adjust test set potentiometer A8R8 until pulse width is 0.5 ± 0.1 µsec at 50% of amplitude.

(c) Perform step 4, and adjust test set potentiometer A8R10 until pulse spacing is 1.8 ± 0.1 µsec.

j. Mode 4 Disparity Adjustment

(1) Test equipment required-Oscilloscope

(2) Adjustment procedure.

NOTE

The following procedure references steps in table 3-13, Mode 4 Disparity Function Test Procedure.

(a) Perform step 1.

(b) Perform step 3, and adjust test set potentiometer A8R14 until pulse on oscilloscope B INPUT is coincident with last pulse on A INPUT, ± 0.1 µsec leading edge to leading edge.

k. SIF Reply Marker Adjustment

(1) Test equipment required-Oscilloscope

(2) Adjustment Procedure. The following procedure references steps in table 3-14, SIF Marker Function Test Procedure.

(a) Perform step 1.

(b) Perform step 5, and adjust test set potentiometer A6R32 until pulse spacing is 20.30 ± 0.02 µsec.

(c) Perform step 6, and adjust test set potentiometer A6R40 until pulse spacing is 24.65 ± 0.02 µsec.

(d) Perform step 7, and adjust test set potentiometer A6R42 until pulse spacing is 4930 ± 0.02 µsec.

l. RF Power Measurement Adjustment

(1) Test equipment required.

(a) Signal Generator

(b) Oscilloscope

(c) RF Power Test Set

(d) Multimeter

(e) Pulse Power Calibrator Set

(f) 10 K ohm resistor

(2) Adjustment procedure

(a) Connect test set up as shown in figure 3-12.

(b) Set up test set per paragraph *3-4a* except DEMOD VID LEVEL shall be fully CCW and MEASUREMENT FUNCTION SELECT to PWR.

(c) Set up signal generator as follows:

1 Adjust FREQUENCY control to 1090 MHZ and ATTENUATI0N (DB) control to 0.00.

2 Set modulation pulse (UPM 15A) into EXT INPUT of Signal Generator with a pulse of +10 volts and a duration of 7 µsec.

3 Set Power level -12 dbm and rf pulse of 0.45 ± 0.1 µsec.

(d) Adjust oscilloscope to view pulses on A INPUT.

(e) Install a 10 K ohm resistor from TP1 to TP2 of M1A1.

(f) Adjust M1A1R1 for 0.00 volts at TP2 of M1A1.

(g) Remove 10K ohm resistor applied in step *(e)* from TP1 and TP2 of M1A1.

(h) Set pulse power Calibrator TRIGGER NO. 1 switch to ON.

(i) Apply -12.0 db into LOW POWER input.

(j) Adjust DEMOD VID LEVEL (R7) for 1.0 VOLT display on oscilloscope.

(k) Adjust M1A1R2 (meter offset) for + 18 dbw on M1 meter.

(l) Apply +3.0 db into LOW POWER input.

(m) Adjust DEMOD VID LEVEL (R-7) for 1.0 volt display on oscilloscope.

(n) Adjust M1A1R7 for +33 dBw on M1 meter.

(o) Repeat steps *(f)* thru *(o)* to assure correct adjustment.

m. PRF Measurement Adjustment

(1) Test equipment required

(a) Oscilloscope

(b) Frequency Counter

(2) Adjustment procedure.

(a) Connect test setup as shown in figure 3-14.

(b) Set test set controls per table 3-1.

(c) Adjust test set PRF SELECT MULT controls until frequency counter indicates 5,000 Hz.

(d) Connect oscilloscope A INPUT to test point A10TP3.

(e) Adjust A10R27 until pulse duration is 99 µsec. See figure 3-3.

(f) Adjust test set PRF SELECT controls until frequency counter indicates 10,000 Hz.

(g) Adjust A10R16 until MEASUREMENT meter indicates 10.0 (10,000 Hz).

(h) Adjust test set PRF SELECT controls until frequency counter indicates 1,000 Hz.

(i) Set MEASUREMENT PRF RANGE switch to Xl00.

(j) Adjust A10R20 until MEASUREMENT meter indicates 10.0 (100 Hz).

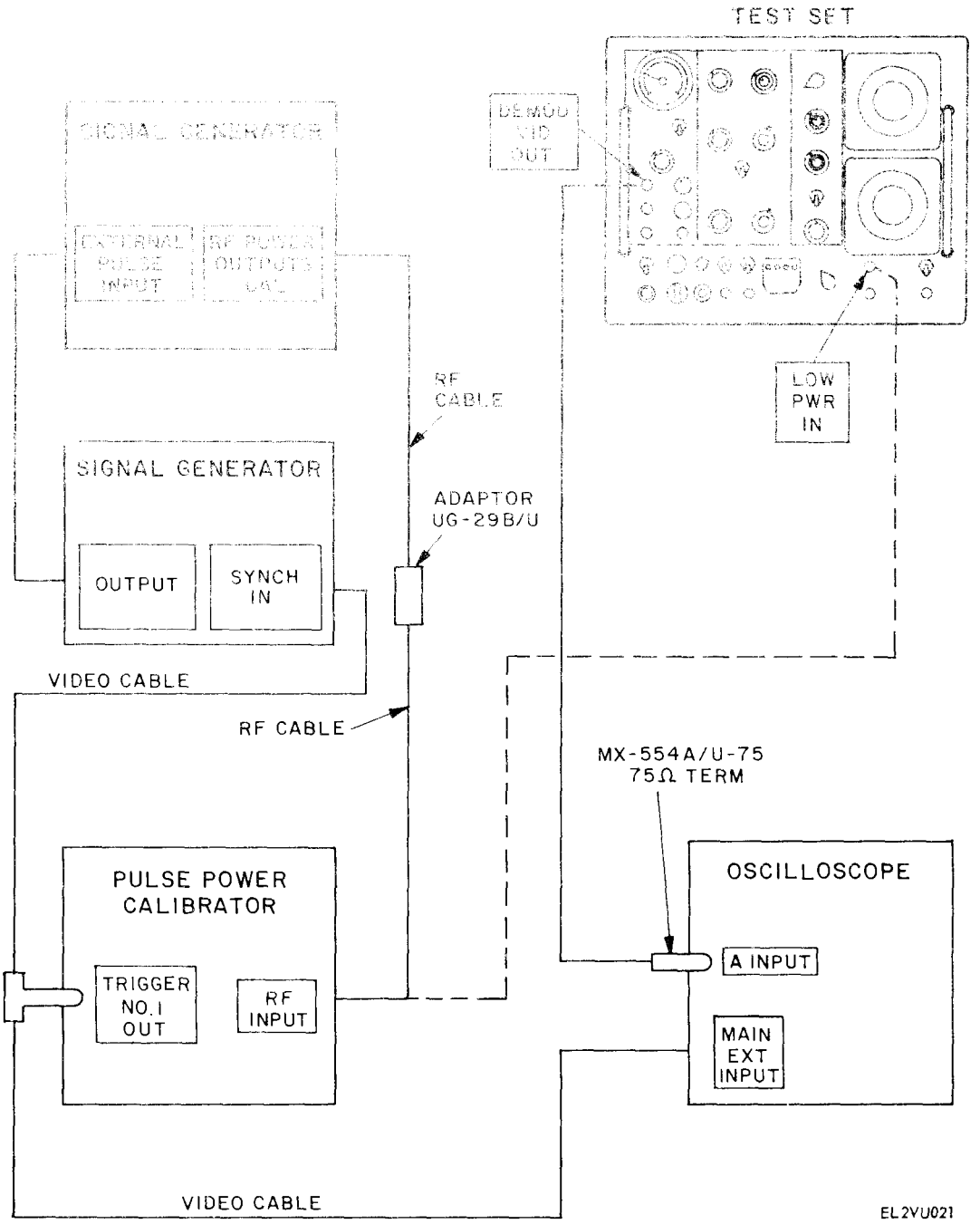


Figure 3-12. Power measurement adjustment setup.

(k) Adjust test set PRF SELECT RANGE controls to X100.

(l) Set MEASUREMENT PRF RANGE switch to X10.

(m) Adjust A10R24 until MEASUREMENT meter indicates 10.0.

n. Marker/Ramp Generator Adjustment

(1) Test equipment required.

(a) Oscilloscope

(b) Digital Voltmeter (dVM)

(c) Transfer Oscillator

(d) Frequency Counter

(e) Square Law Detector

(f) R.F. Power Meter

(g) Comparator Frequency

(2) Adjustment procedure (ramp generator) A11A1.

(a) Connect test setup as shown in figure 3-15.

(b) Connect oscilloscope MAIN EXT INPUT jack to test set MEASUREMENT SCOPE TRIG OUT J7, and A INPUT to TPF-7 (positive gate).

(c) Set SIG GEN FCTN switch to SWP ± 5 MHz.

(d) Set oscilloscope DISPLAY to switch A and adjust sweep controls to view one complete ramp signal (TPF-7)

(e) Set A11A1R82 to fully CCW position.

(f) Adjust A11A1R80 until ramp signal is 780 µsec duration.

(g) Set SIG GEN FCTN switch to SWP ± 20 MHz.

(h) Adjust A11A1R79 for 2200 µsec duration.

(i) Remove Oscilloscope probe from TPF-7 and connect to TPF-6 (ramp out).

(j) Adjust the D.C. Level of the ramp out with A11A1R73 for 0.0 volts.

(k) Set SIG GEN FUNCTION to SWP ±5 MHZ; adjust the ramp voltage of ramp out for -1.2V to +1.2V using A11A2R74.

(l) Set SIG GEN FCTN switch to SWP ± 20 MHz.

(m) Adjust ramp voltage of ramp out for -2.0 volts to +2.0 volts using A11A1R66.

(n) Connect test set up as in figure 3-24.

(o) Set SIG GEN FUNCTION switch to SWP ± 5 MHZ and CHAL MODE SELECT switch to CW.

(p) Adjust A11A1R2 for -10 dbm at AUX OUT jack with attenuator set to -10 db.

(q) Set SIG GEN FCTN switch to FIXED FREQ.

(r) Power meter should be less than ± 0.5 dbm of reading in step *(p).*

(s) Remove cable from Test Set AUX RF IN/OUT and connect to MAIN RF IN/OUT jack.

(t) Set SIG GEN FUNCTION from FIXED FREQ to SWP ± 5 MHZ.

(u) Power meter should be less than ± 0.5 dbm of reading in step *(p).*

(v) Connect test setup as shown in figure 3-23.

(w) Setup test set per paragraph 3-4a and as follows:

CHAL MODE SELECT	CW
SIG GEN FCTN	SWP ±20 MHz

(x) Adjust transfer oscillator FREQUENCY (MHz) control until zero beat is aligned with leading edge of 1st marker.

(y) Set oscilloscope sweep display and adjust until first marker (-20 MHz) is centered on oscilloscope display.

(z) Readjust transfer oscillator FREQUENCY (MHz) control until zero beat is aligned with leading edge of marker.

(aa) Adjust A11A1R6 until frequency of leading edge of marker is 1009.7 to 1010.3 MHz.

(ab) Set oscilloscope sweep display switch to MAIN.

(ac) Adjust transfer oscillator FREQUENCY (MHz) control to align zero beat with each of the markers listed below and repeat steps *(q)* through *(w)* while adjusting as listed below.

Marker	*Frequency*	*Adjust*
2 (-5 MHz)	1024.9 to 1025.1 MHz	A11A1R11
3 (-3 MHz)	1026.9 to 1027.1 MHz	A11A1R16
4 (-1 MHz)	1028.9 to 1029.1 MHz	A11AR21
5 (0)	1029.9 to 1030.1 MHz	A11A1R26
6 (+ 1MHz)	1030.9 to 1031.1 MHz	A11A1R31
7 (+3 MHz)	1032.9 to 1033.1 MHz	A11A1R36
8 (+5 MHz)	1034.9 to 1035.1 MHz	A11A1R41
9 (+20 MHz)	1049.7 to 1050.3 MHz	A11A1R46

o. Timing Marker Output Adjustment

(1) Test equipment required-Oscilloscope

(2) Adjustment procedure.

(a) Connect test setup as shown in figure 3-28.

NOTE

The following procedure references steps in Table 3-20 Timing Marker Function Test Procedure.

(b) Perform Step *1a,* and adjust A9R14 until pulse on oscilloscope A INPUT is 2.5 ± 0.3 volts.

(c) Perform Step *1b,* and adjust A9R13 until Pulse on oscilloscope A INPUT is 1.7 ± 0.2 volts.

(d) Perform step *1c,* and adjust A9R12 until pulse on oscilloscope A INPUT is 1.0 ± 0.2 volts.

3-11. Alignment Procedure.

Alignment procedure are not required.

Section V. REPAIR

3-12. Parts Replacement Techniques.

All pints are easily accessible and can be replaced without special procedures. The following general precautions apply to the equipment:

a. Use the pencil type 55-watt soldering iron supplied with Toolkit, Electronic Equipment TK-105/G for removal and repair of chassis mounted components. If the iron is to be used with alternating current, use an isolating transformer between the soldering iron and the line. Do not use a soldering gun; damaging voltages can be induced in components.

b. When soldering transistor or diode leads, solder quickly; whenever wiring permits, use a heatsink (such as long-nosed pliers) between the soldered joint

and the transistor or diode. Use approximately the same lead length and dress as used originally.

c. Wiring diagram information and cable diagrams in figure FO-13 and parts location information in figures 3-2 through 3-10 should be referred to as required to ensure correct part replacements.

d. Filter Assembly A13 Repair. Filter assembly A13 is to be repaired in accordance with the following procedure.

(1) Remove dust cover, and control panel from test set as described in paragraphs 3-8a, and *3-8i.*

(2) Remove four screws securing filter assembly A13 to control panel.

(3) Tag and unsolder external connections of filter assembly A13.

(4) Remove filter assembly A13 from control panel.

(5) Remove six screws, plate and gasket from side of filter assembly A13.

(6) Remove nuts, washer, and terminal lug securing filter A13FL1 and A13FL2 in place. (Nuts, washer, and terminal are located on outside of filter assembly.)

(7) Without disturbing relative position of parts withdraw electrical components of filter assembly A13. The electrical components consist of jack A13, filters A13FL1 and A13FL2, and resistors A13R1 and A13R2 (see FO-13, Detail A, sheet 2).

(8) Replace defective component. (If necessary refer to schematic FO-11, sheet 2).

(9) Reinstall electrical components in filter assembly.

(10) Secure filters A13FL1 and A13FL2 to filter assembly A13 using nuts, washer, and terminal lug removed in step *(6).*

(11) Make sure parts are positioned as shown in figure FO-13, Detail A.

(12) Replace filter assembly in control panel and reconnect external connections.

(13) Replace control panel, and dust cover of test set as described in paragraphs *3-9b,* and *3-9j.*

3-13. Parts Substitution.

Do not substitute parts indiscriminately. Substitute parts only when the trouble has been isolated to a specific stage and the defective part has been localized.

Section VI. FUNCTION TEST PROCEDURES

3-14. Purpose and Instructions.

a. Test procedures in table 3-2 to be used for general support maintenance to determine the acceptability of repaired equipment unless the fault was noted during function test. If the fault was noted during function test the tables in this section are to be used to determine the acceptability of repaired equipment. These procedures set forth specific requirements that repaired equipment must meet before it is returned to the using organization.

b. Separate function test procedures are given to check various sections of the test set so that only the section repaired is tested. Performing all tests in the order given will provide a complete test of the test set should it be required.

c. Perform each function test procedure in sequence; do not vary the sequence, For each step, perform all the actions required in the Control setting column; then perform specific test procedure and verify it against the performance standard.

3-15. Test Equipment Required for Testing

All test equipment required to perform the testing procedures of this section is listed in TM 11-6625-2611-12. Power input connections to the test set and the test equipment are not shown on the test setup figures unless power input is part of test procedure.

3-16. Test Procedures.

Function test procedures are listed in table 3-4.

Table 3-4. List of Function Test Procedures

Test	Table No.
Power supply and overall test procedure	3-5
Internal prf frequency function test procedures	3-6
PRF measurement accuracy function test procedures	3-7
Output trigger function test procedures	3-8
Challenge code function test procedures	3-9
ISLS function test procedures	3-10
Suppressor pulse function test procedures	3-11
Mode 4 interface input and output function test procedures	3-12
Mode 4 disparity function test procedures	3-13
SIF reply marker function test procedures	3-14

Table 3-4. List of Function Test Procedures- Continued

Test	Table No
Output rf frequency function test procedures	3-15
RF power output function test procedures	3-16
Modulator and demodulator function test procedures	3-17
Input power measurement function test procedures	3-18
Frequency measurement function test procedures	3-19
Timing marker function test procedures	3-20

Table 3-5. Power Supply and Overall Test Procedure

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
1		POWER switch OFF	Inspect all controls and mechanical assemblies for loose or missing screws, nuts, and bolts.	Screws, nuts, and bolts must be tight; none missing.
2			Inspect all connectors, sockets, and receptacles for looseness and damage.	No looseness or damage evident.
3			Inspect plugs, connectors, control knobs, and control unit for cleanliness.	All items must be free of dust or dirt. If cleaning is required, refer to TM 11-6625-2611-12.
4			Inspect all cable assemblies for signs of mechanical damage, such as chafed, cracked, or frayed insulation.	All cables must be free of chafed, cracked, and frayed insulation
5			Inspect gaskets of control unit case for looseness, deterioration or damage.	Observe that all gaskets are tight, resilient, and free from cuts or tears.
6	Connect test setup as shown in figure 3-13.	POWER switch OFF SIG GEN FCTN switch SWP ±20 MHZ CHAL MODE SELECT switch C	Adjust transformer until voltmeter indicates 115 vat.	
		POWER switch ON	a. Observe POWER 1.0 AMP fuseholder.	a. Fuseholder is extinguished.
			b. Observe POWER indicator.	b. POWER indicator is lit.
			C. Observe POWER DC FAULT indicator.	POWER DC FAULT indicator is extinguished.
			d. Activate POWER DC FAULT indicator.	d. POWER DC FAULT indicator lights.
			a. Connect differential voltmeter between PS1A1TP1 (+) and ground. Observe differential voltmeter indication.	Differential voltmeter indicates 27.75 to 28.25 volts.
			b. Adjust transformer until multimeter indicates 103.5 volts. Using procedure followed in step a, obtain differential voltmeter indication.	b. Differential voltmeter indicates 27.75 to 28.25 volts.
			c. Adjust transformer until multimeter indicates 126.5 volts.	Differential voltmeter indicates 27.75 to 28.5 volts.

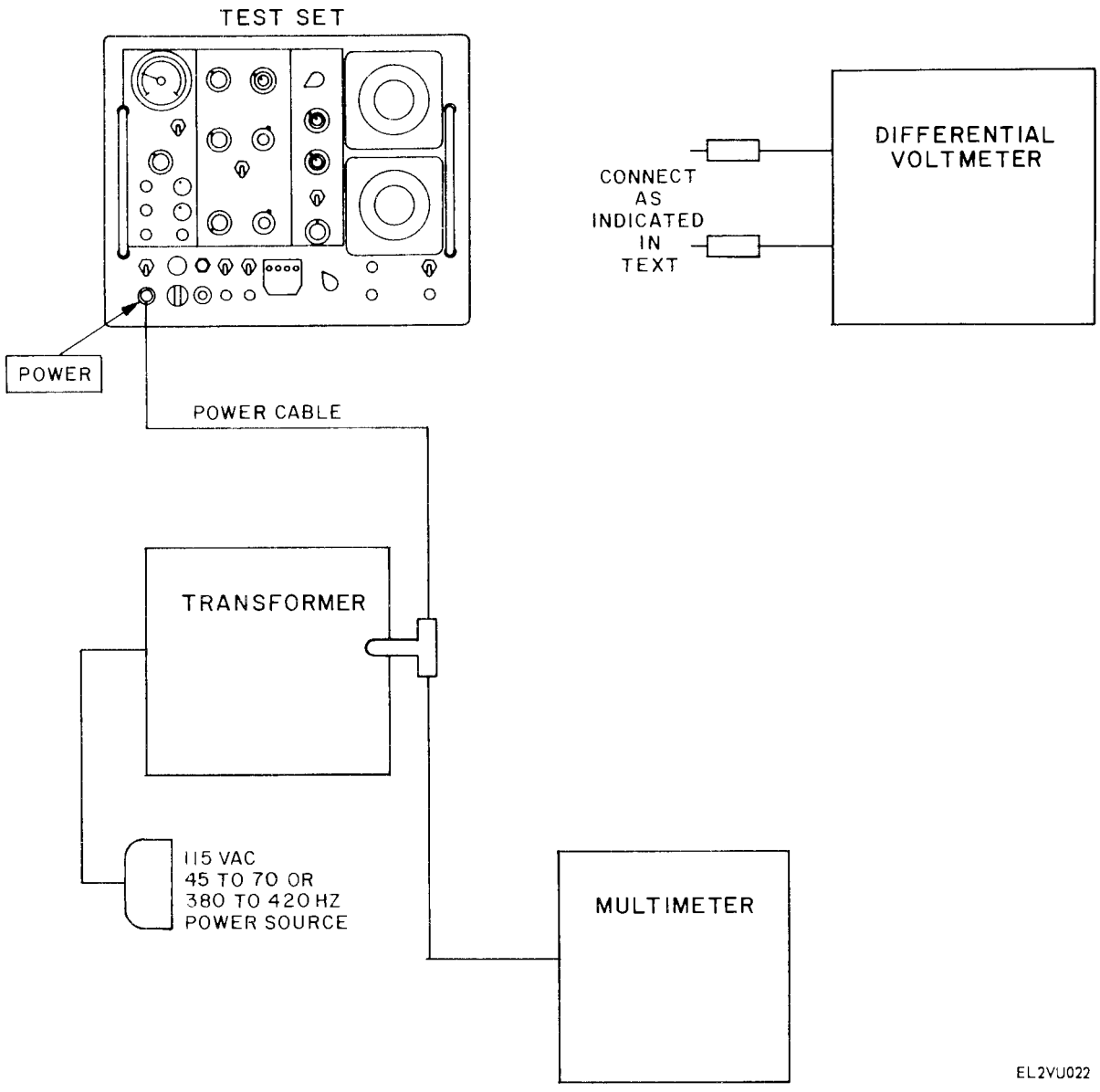


Figure 3–13. Power Supply Test Setup

Table 3-5. Power Supply and Overall Test Procedure—Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
9			a. Connect differential voltmeter between PS141TP5 (+) and ground.	a. Differential voltmeter indicates 11.75 to 12.25 volts.
10			a. Connect differential voltmeter between PS1A1TP6 (-) and ground.	a. Differential voltmeter indicates 11.75 to 12.25 volts.
			b. Adjust transformer until multimeter indicates 126.5 volts.	b. Differential voltmeter indicates 11.75 to 12.25 volts.
11			a. Connect differential voltmeter between PS1A1TP7 (+) and ground.	a. Differential voltmeter indicates 4.75 to 5.25 volts.
			b. Adjust voltmeter until multimeter indicates 103.5 volts.	b. Differential voltmeter indicates 4.75 to 5.25 volts.

Table 3-6. Internal Prf Frequency Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1		Set per paragraph 3-4a and as follows: PRF SELECT MULT control 1.00.	Connect test setup as shown in figure 3-14. Observe frequency counter indication.	0.900 to 1.100 KC
2		PRF SELECT MULT control 11.00	Observe frequency counter indication.	10,500 to 11.500 KC
3		PRF SELECT RANGE switch X100.	Observe frequency counter indication.	1.050 to 1.150 KC
4		PRF SELECT MULT control 1.00.	Observe frequency counter indication.	0.090 to 0.120 KC
5		PRF SELECT RANGE switch Xl0.	Observe frequency counter indication.	0.010 to 0.011 KC
6		PRF SELECT MULT control 11.00	Observe frequency counter indication.	0.110 to 0.120 KC

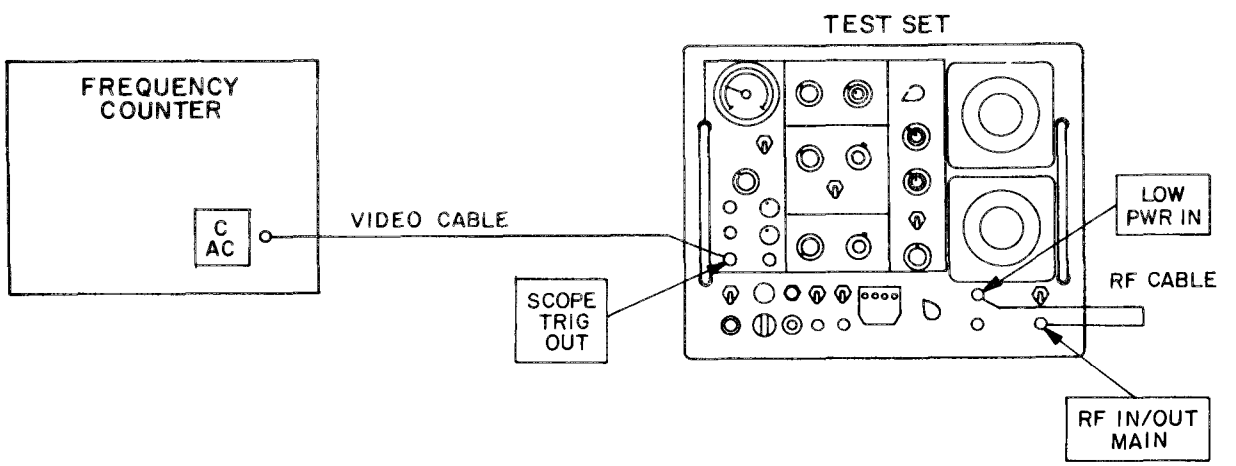


Figure 3-13. Power supply test setup

Table 3-7. PRF Measurement Accuracy Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1		Set per paragraph 3-4a and as follows: PRF SELECT RANGE switch X10 MEASUREMENT PRF RANGE switch X10	Connect test setup as shown in figure 3-14. Adjust PRF SELECT MULT control until MEASUREMENT meter indicates 1.5. Observe frequency counter indication.	Frequency counter indication is 0.0135 to 0.0165 KC
2			Adjust PRF SELECT MULT control until MEASUREMENT meter indicates 10.0. Observe frequency counter indication.	Frequency counter indication is 0.095 to 0.105 KC
3		MEASUREMENT PRF RANGE switch: X100.	Adjust PRF SELECT MULT control until MEASUREMENT meter indicates 1.0. Observe frequency counter indication.	Frequency counter indication is 0.090 to 0.110 KC
4		PRF SELECT RANGE switch X100.	Adjust PRF SELECT MULT control until MEASUREMENT meter indicates 10.0. Observe frequency counter indication.	Frequency counter indication is 0.950 to 1.050 KC
5		MEASUREMENT PRF RANGE switch X1K	Adjust PRF SELECT MULT control until MEASUREMENT meter indicates 1.0. Observe frequency counter indication.	Frequency counter indication is 0.900 to 1.100 KC
6		PRF SELECT switch X1K.	Adjust PRF SELECT MULT control until MEASUREMENT meter indicates 10.0. observe frequency counter indication.	Frequency counter indication is 9.500 to 10.500 KC

Table 3-8. Output Trigger Function Test Procedure

Step No.	Control Settings		Test procedure	performance standard
	Test equipment	Test set		
1		Setup test set per paragraph 3-4a and as follows: PRF SELECT MULT control 1.0.	Connect test setup as shown in figure 3-15; observe pulse amplitude and duration. (A Channel)	Pulse amplitude 4.0 to 6.0 volts. (A Channel) Pulse duration 1 to 5 μsec.
2		SCOPE TRIG/FREQ MEAS DELAY (μSEC) RANGE switch X0.4.	Adjust test set SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control to center pulse leading edge on oscilloscope display.	Pulse rise time is less than 0.1 μsec.
		SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control 10.0	Adjust oscilloscope A INPUT VOLTS/DIV vernier control a pulse amplitude of 8 divisions. Using oscilloscope CRT graticule, measure distance in divisions between 10% and 90% amplitude points.	

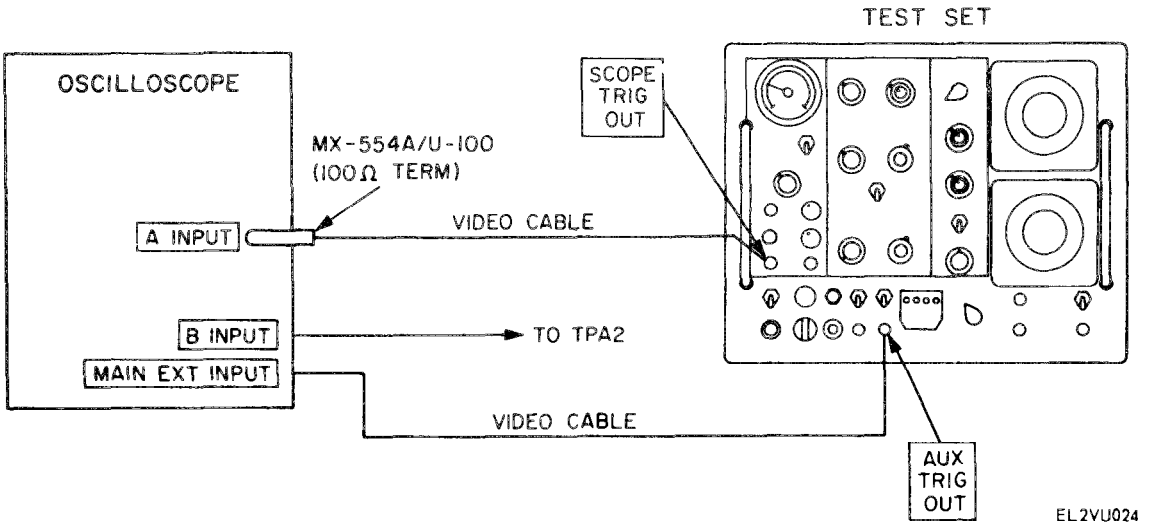


Figure 3-15. Scope output trigger test setup

Table 3-8. Output Trigger Function Test Procedure—Continued

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
2. (Cont)			**NOTE** The two exterior dotted horizontal lines on CRT graticule are 10% and 90% amplitude points. Multiply distance in divisions by setting of MAIN TIME/DIV switch to obtain rise and fall times.	
3			Adjust test set SCOPE TRIG/ FREQ MEAS DELAY (µSEC) MULT control ccw to center pulse falling edge. Repeat procedure of step 2 to measure pulse fall time.	Pulse fall time is less than 0.5 µsec.
4			Connect test setup as shown in Figure 3-16.	Pulse amplitude 17 to 23 volts.
			Observe pulse amplitude and duration.	Pulse duration 1.0 ±0.5 µsec.
5			Using same procedure as in step 2, measure pulse rise and fall times.	Pulse rise time is less than 0.1 µsec. Pulse fall time is less than 0.2 µsec.
6		SCOPE TRIG FREQ MEAS DELAY (µSEC) RANGE switch OFF	Connect oscilloscope B INPUT probe to TPA5 (figure 3-1)(0 trig.) Measure delay between leading edges of signals on B and A INPUTS.	Delay is 4.0 ±1.0 µsec.

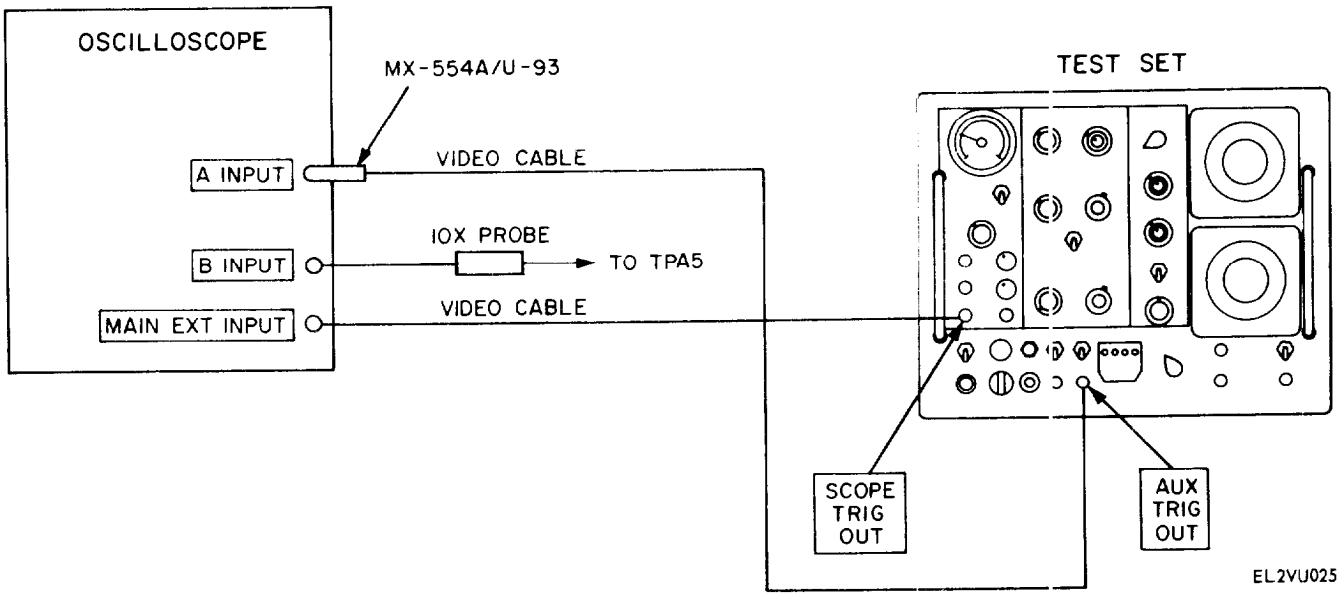


Figure 3–16. Auxiliary trigger test setup

Table 3–8. Output Trigger Function Test Procedure—Continued

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
7		SIG GEN FCTN switch SWP ±5 MHZ	Connect oscilloscope B INPUT probe to TPA2 (rawdly trig).	
		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X4	Observe pulses.	Leading edge of pulse on A INPUT is within 0.5 µsec. of trailing edge of pulse on B INPUT
		SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 1.0.		
8		AUX TRIG switch OFF	Observe oscilloscope	Pulse on A INPUT disappears.
9		SIG GEN FCTN switch FIXED FREQ	Connect test setup as shown in Figure 3-15.	
		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X0.4.	Note delay betwen leading edges of signals on A and B INPUTS.	
		AUX TRIG switch ON		
10		SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 1.0	Measure delay between leading edges of signals on A and B INPUTS.	Signal is delayed 0.3 to 0.5 usec.
		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X0).4		
11		SCOPE TRIG/FREQ MEAS DELAY (µSEC) MULT control 11.0	Measure delay between leading edges of signals on A and B INPUTS.	Delay is 4.0 to 4.8 µsec.
12		SCOPE TRIG/FREQ MEAS DELAY (µSEC) RANGE switch X4.	Measure delay between leading edges of signals on A and B INPUTS.	Delay is 40 to 48 µsec.

Table 3-8. Output Trigger Function Procedure - Continued

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
13		SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control 1.0	Measure delay between leading edges of signals on A and B INPUTS.	Delay 3.6 to 4.4 μsec.
14		SCOPE TRIG/FREQ MEAS DELAY (μSEC) RANGE switch X40	Measure delay between leading edges of signals on A and B INPUTS.	Delay is 36 to 44 μsec.
15		SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control 11.0 PRF SELECT RANGE switch X100	Measure delay between signals on A and B INPUTS.	Delay is 400 to 480 μsec.
16		SCOPE TRIG/FREQ MEAS DELAY (μSEC) RANGE switch X400	measure delay between signals on A and B INPUTS.	Delay is 4000 to 4800 μsec.
17		SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control 10.0	Using oscilloscope DIV DELAY control locate pulse on A INPUT. Measure pulse jitter.	Jitter is less than 0.41 μsec.
18		SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control 1.0	Measure delay between signals on A and B INPUTS.	Delay is 360 to 440 μsec.
19		SCOPE TRIG/FREQ MEAS DELAY (μSEC) RANGE switch X0.4 SCOPE TRIG/FREQ MEAS DELAY (μSEC) MULT control 1.25 PRF SELECT RANGE switch X1K.	Using oscilloscope HORIZONTAL POSITION controls locate leading edge of pulse on A INPUT. Measure pulse jitter.	Less than 0.01 μsec.

Table 3-9. Challenge Code Function Test Procedure

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
1	Apply 1.0 μsec. signal from time mark generator.	Set up test set per paragraph 3-4*a*.	Connect test set up as shown in figure 3-17. Observe two pulses are displayed on oscilloscope. Determine spacing between leading edges of pulses as follows: a. Adjust HORIZONTAL POSITION control to display 1st pulse only. b. Set DISPLAY switch to ALT c. Set HORIZONTAL MAGNIFIER switch to X10. d. Adjust A and B POSITION controls so that a peak of a 0.1 μsec marker cycle (B INPUT) intersects leading edge of a A INPUT pulse. e. Adjust HORIZONTAL position control ccw to display 2nd pulse.	Pulse spacing is 3.0 ±0.05 μsec.

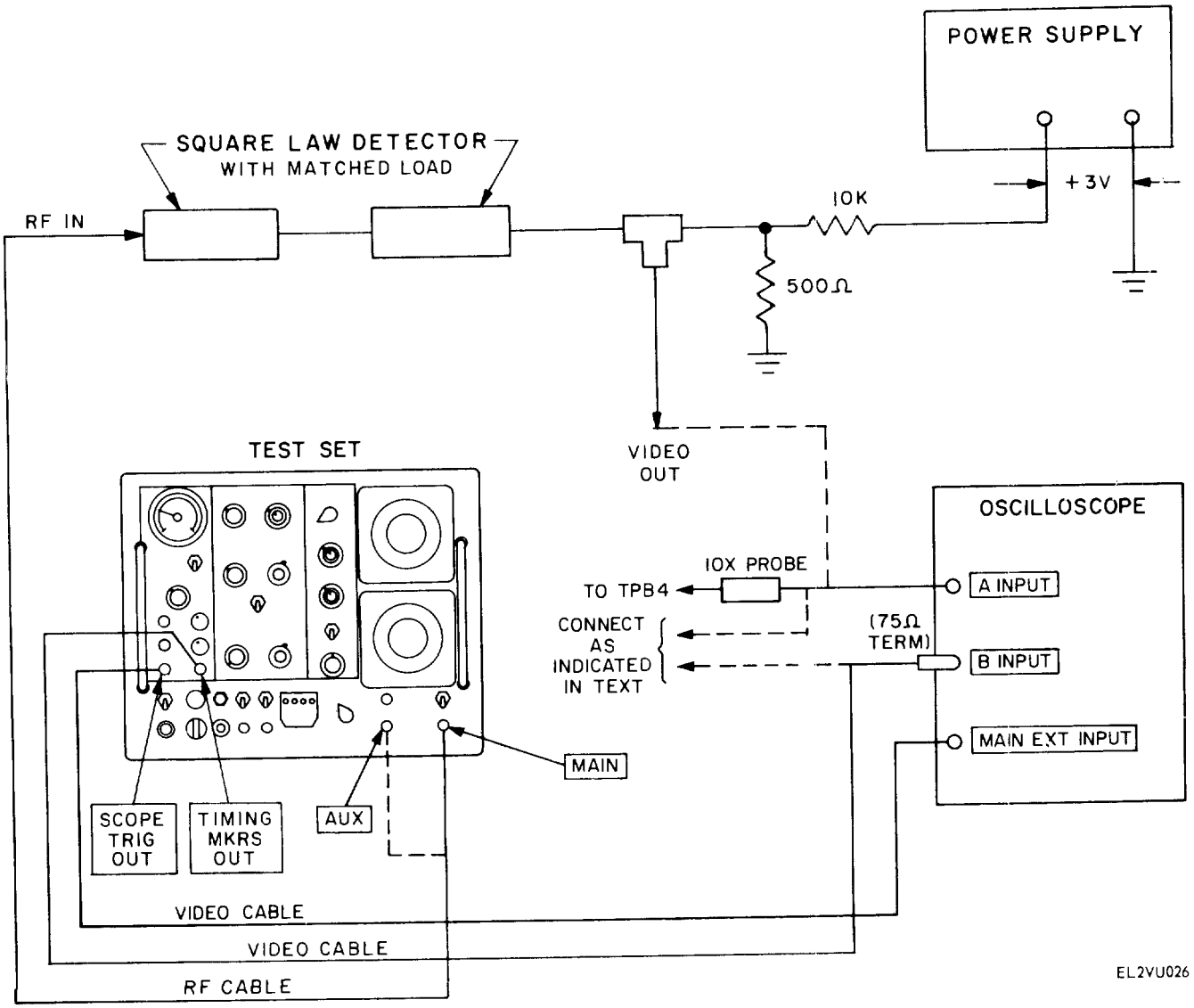


Figure 3-17. Challenge code test setup

Table 3-9. Challenge Code Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
2		CHAL SUB PULSE POSITION SELECT switch -.9	Measure pulse spacing.	Pulse spacing is 3.9 ±0.05 μsec.
3		CHAL SUB PULSE POSITION SELECT switch -.2	Measure pulse spacing.	Pulse spacing is 3.2 ±0.05 μsec.
4		CHAL SUB PULSE POSITION SELECT switch +.2	Measure pulse spacing.	Pulse spacing is 2.8 ±0.05 μsec.
5		CHAL SUB PULSE POSITION SELECT switch +.9	Measure pulse spacing.	Pulse spacing is 2.1 ±0.05 μsec.

Table 3-9. Challenge Code Function Test Procedure - Contineud

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
6		CHAL SUB PULSE POSITION SELECT switch VARY	Adjust CHAL SUB PULSE POSITION VARY control through entire range. Observe pulse spacing.	Pulse spacing varies from less than 2.0 μsec. to more than 4.0μsec.
7		CHAL MODE SELECT switch 2 CHAL SUB PULSE POSITION SELECT switch +.9	Measure pulse spacing.	Pulse spacing is 4.1 ±0.05 μsec.
8		CHAL SUB PULSE POSITION SELECT switch 0.	Measure pulse spacing.	Pulse spacing is 5.0 ±0.5 μsec.
9		CHAL MODE SELECT switch 3/A	Measure pulse spacing.	Pulse spacing is 8.0 ±0.05 μsec.
10		CHAL SUB PULSE POSITION SELECT switch +.9	Measure pulse spacing.	Pulse spacing is 7.1 ±0.05 μsec.
11		CHAL MODE SELECT switch C	Observe two pulses are displayed on oscilloscope.	Pulse spacing is 20.1 ±0.05 μsec.
12		CHAL SUB PULSE POSITION SELECT switch 0	Measure pulse spacing.	Pulse spacing is 21.0 ±0.05 μsec.
13		CHAL MODE SELECT switch TEST	Measure pulse spacing.	Pulse spacing is 6.50 ±0.05 μsec.
14		CHAL SUB PULSE POSITION SELECT switch +.9	Measure pulse spacing.	Pulse spacing is 5.6 ±0.05 μsec.
15		CHAL MODE SELECT switch 4A CHAL WIDTH SELECT switch 0.50 PRF SELECT X-1/2	Observe number of pulses in challenge pulse word.	28 pulses present.
16		CHAL SUB PULSE SELECT switch M4P2	Observe second pulse of train.	Second pulse moves out of position.
17		CHAL SUB PUSLE SELECT switch M4P3	Observe third pulse of train.	Second pulse returns to original position and third pulse moves out of position.
18		CHAL SUB PULSE SELECT switch M4P4	Observe fourth pulse of train.	Third pulse returns to original position and fourth pulse moves out of position.
19		CHAL SUB PULSE POSITION SELECT switch 0	Adjust oscilloscope MAIN VERNIER control until 28 pulses are displayed within CRT graticule. Observe that pulses are present at 0, 2, 4, 6, 10, 13, 15, 17, 20, 24, 26, 30, 33, 35, 38, 41, 43, 45, 48, 50, 52, 54, 58, 61, 63, 66, 68, and 71, μsec. positions, then measure spacing between first and last pulse. a. Markers are now 1 μsec. apart. b. Count number of 0.1 μsec markers from 70 μsec reference point to leading edge of last pulse. Multiply count by 0.1 and add to 70 for final measurement.	Pulse spacing is 71 ±0.07 μsec.

Table 3-9. Challenge Code Function Test Procedure—Continued

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
20		CHAL MODE SELECT switch 4B	Observe number of pulses in challenge word,	28 pulses present.
21			Observe that pulses are present at 0, 2, 4, 6, 10, 12, 15, 17, 19, 22, 25, 28, 30, 32, 35, 37, 40, 44, 48, 51, 53, 55, 57, 60, 62, 64, 66, and 70μsec positions, then measure spacing between first and last pulse, and repeat step 19.	Pulse spacing is 70 ±0.07 μsec.
22		CHAL MODE SELECT switch 1. CHAL WIDTH SELECT switch 0.80 PRF SELECT Xl	Connect square law detector to test set RF IN/OUT MAIN jack and oscilloscope A INPUT as shown in figure 3-17. Observe two pulses are present. Adjust oscilloscope DIV DELAY control to position intensified trace over 2nd challenge pulse,	
23			Using 0.1 μsec markers measure pulse width at 50% amplitude points.	Pulse width is 0,80 ±0.05 μsec.
24			Measure pulse rise time between 1% and 81% amplitude points. Multiply distance in divisions between two points by setting of DELAYED TIME/DIV switch to obtain rise time.	Pulse rise time is 0.05 to 0.10 μsec.
25			Using procedure outlined in step 24, measure pulse fall time.	Pulse fall time is 0.05 to 0.20 μsec.
26		CHAL WIDTH SELECT switch 0.25	Using 0.1 μsec. markers, measure pulse width at 50% amplitude points	Pulse width is 0.25 ±0.05 μsec.
27		CHAL WIDTH SELECT switch 0.50	Using 0.1 μsec. markers, measure pulse width at 50% amplitude points	Pulse width is 0.5 ±0.05 μsec.
28		CHAL WIDTH SELECT switch 1.70	Using 0.1 μsec. markers, measure width at 50% amplitude points,	Pulse width is 1.70 ±0.05 μsec.
29		CHAL WIDTH SELECT switch VARY	Vary CHAL WIDTH VARY control throughout entire range and measure pulse width at min. and max.	Pulse width varies from less than 0.25 to more than 1.7 μsec.
30		CHAL WIDTH SELECT switch 0.80	Disconnect input of square law detector from test set RF lN/OUT MAIN jack and connect to RF IN/OUT AUX jack; repeat steps 22 through 29 for aux channel.	
31		CHAL AUX MOD DLY control 0.2 μSEC	Connect oscilloscope A INPUT to TPB4 and B INPUT to TPB3. Measure delay from leading edge of first A INPUT pulse to leading edge of first B INPUT pulse.	Delay is 0.2 ±0.05 μsec.

Table 3-9. Challenge Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
32		CHAL AUX MOD DLY control .05 μSEC	Measure delay from leading edge of first A INPUT pulse to leading edge of first B INPUT pulse.	Delay is 0.05 μsec or less.
33		CHAL AUX MOD DLY control 0.4 μSEC	Measure delay from leading edge of first A INPUT pulse to leading edge of the first B INPUT pulse.	Delay is 0.4 μsec or greater.

Table 3-10. ISLS Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Set up oscilloscope	Set up test per paragraph 3-4*a* except as noted below: CHAL INHIB switch ISLS ON MEASUREMENT FUNCTION SELECT switch PRF CHAL CHAL WIDTH SELECT switch 0.25.	Connect test setup as shown in figure 3-18; observe three pulses are displayed. Measure spacing from leading edge to leading edge of first two pulses.	Pulse spacing is 2 ± 0.05 μsec.
2			Adjust oscilloscope HORIZONTAL POSITION control to center 2nd pulse on display. Using the 0.1 μsec markers, measure pulse width at 50% amplitude points.	Pulse width is 0.8 ± 0.05 μsec.
3		CHAL MODE SELECT switch 4A PRF SELECT X-1/2	Adjust oscilloscope MAIN VERNIER control to display 29 pulses. Adjust oscilloscope DIV DELAY control to position intensified trace over 5th pulse (ISLS), and set sweep display switch to DELAYED. Use 0.1 μsec markers to measure pulse width of 5th pulse at 50% amplitude points.	Pulse width is 0.5 ± 0.05 μsec.
4			Measure pulse spacing from leading edge of 1st to 5th pulse.	Pulse spacing is 8 ± 0.07 μsec.
5			Vary setting of test set AUX ATTEN control while observing oscilloscope.	Fifth pulse is only pulse which varies in amplitude.
6		CHAL ISLS SPACING SELECT switch -.60 CHAL MODE SELECT switch 1	Measure pulse spacing from leading edge of 1st to 2nd pulse.	Pulse spacing is 1.40 ± 0.05 μsec

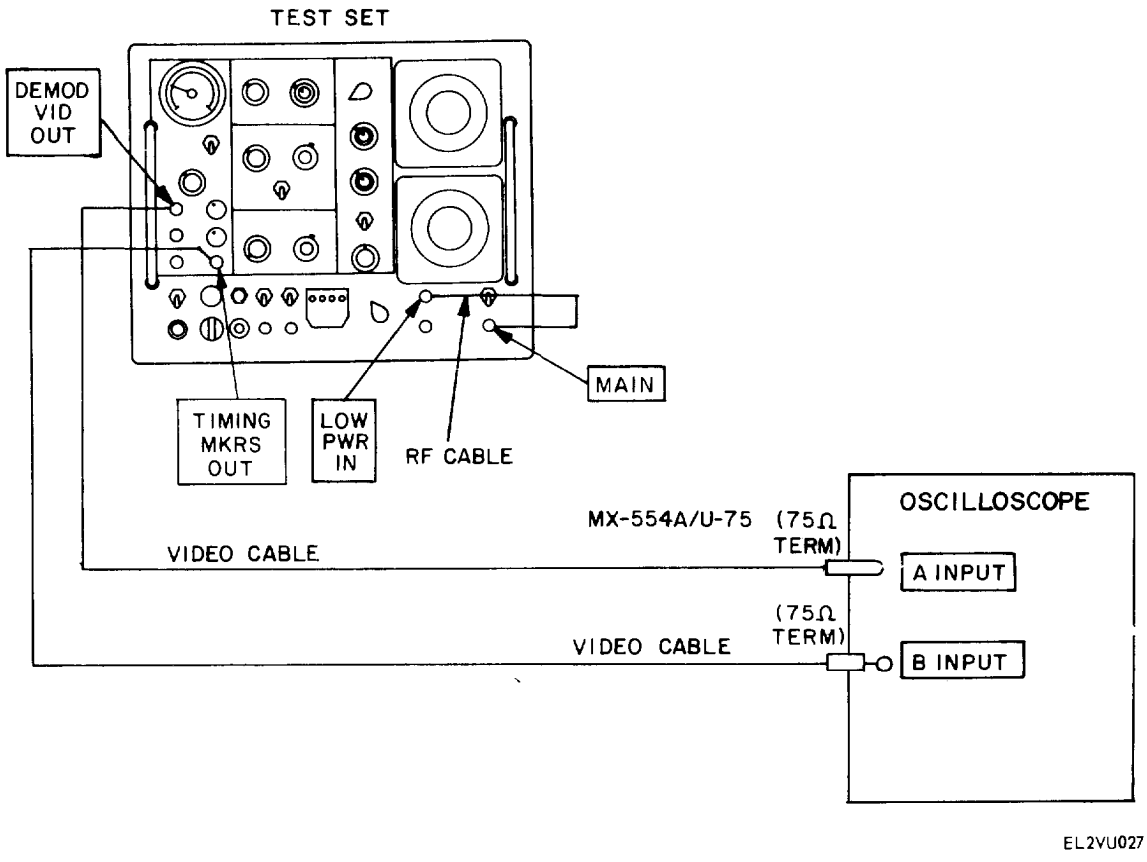


Table 3-10. ISLS Function Test Procedure-Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
7		CHAL ISLS SPACING SELECT switch -.15	Measure pulse spacing fron leading edge of 1st to 2nd pulse.	Pulse spacing is 1.85 ± 0.05 μsec.
8		CHAL ISLS SPACING SELECT switch +.15	Measure pulse spacing fron leading edge of 1st and 2nd pulse.	Pulse spacing is 2.15 ± 0.05 μsec.
9		CHAL ISLS SPACING SELECT switch +.60	Measure pulse spacing fron leading edge of 1st and 2nd pulse.	Pulse spacing is 2.60 ± 0.05 μsec.
10		CHAL ISLS SPACING SELECT switch VARY	Vary CHAL ISLS SPACING VARY control throughout entire range and measure pulse spacing at control extremes	Pulse spacing can be varied from less than 1.0 to more than 3.0 μsec.
11	Oscilloscope DISPLAY switch A		Disconnect cable from RF IN/OUT MAIN jack and connect to RF IN/(OUT jack.	No signal displayed on oscilioscope.
12		CHAL INHIB switch OFF		Two pulses displayed on Oscilloscope.

Table 3-11. Suppressor Pulse Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Set up oscilloscope	Set up test set per paragraph 3–4*a*	Connect test set up as shown in figure 3–19. Measure amplitude of pulse on A INPUT	Pulse is 20 ±2 volts.
2			Measure width of pulse on A PUT	Pulse width is 30 ±3 μsec.
3			a. Measure and note A INPUT pulse time duration between 10% and 90% amplitude points.	a. Pulse rise is 20 v/μsec or greater.
			b. Measure and note A INPUT pulse amplitude between 10% and 90% points.	b. Same as *a* above.
			c. Divide measurement in step b by measurement in step *a* to obtain pulse rise time in v/μsec.	c. Same as *a* above.
4			Adjust oscilloscope DIV DELAY control to center falling edge of A INPUT pulse. Repeat procedure in step 3 to measure pulse fall time.	Pulse fall time is 20 v/μsec or or greater.
5			Measure spacing between leading edges of pulses on A and B INPUT.	Pulse spacing is less than 1.0 μsec.
6		SUPPR switch OFF Observe oscilloscope.		Pulse on A INPUT disappears

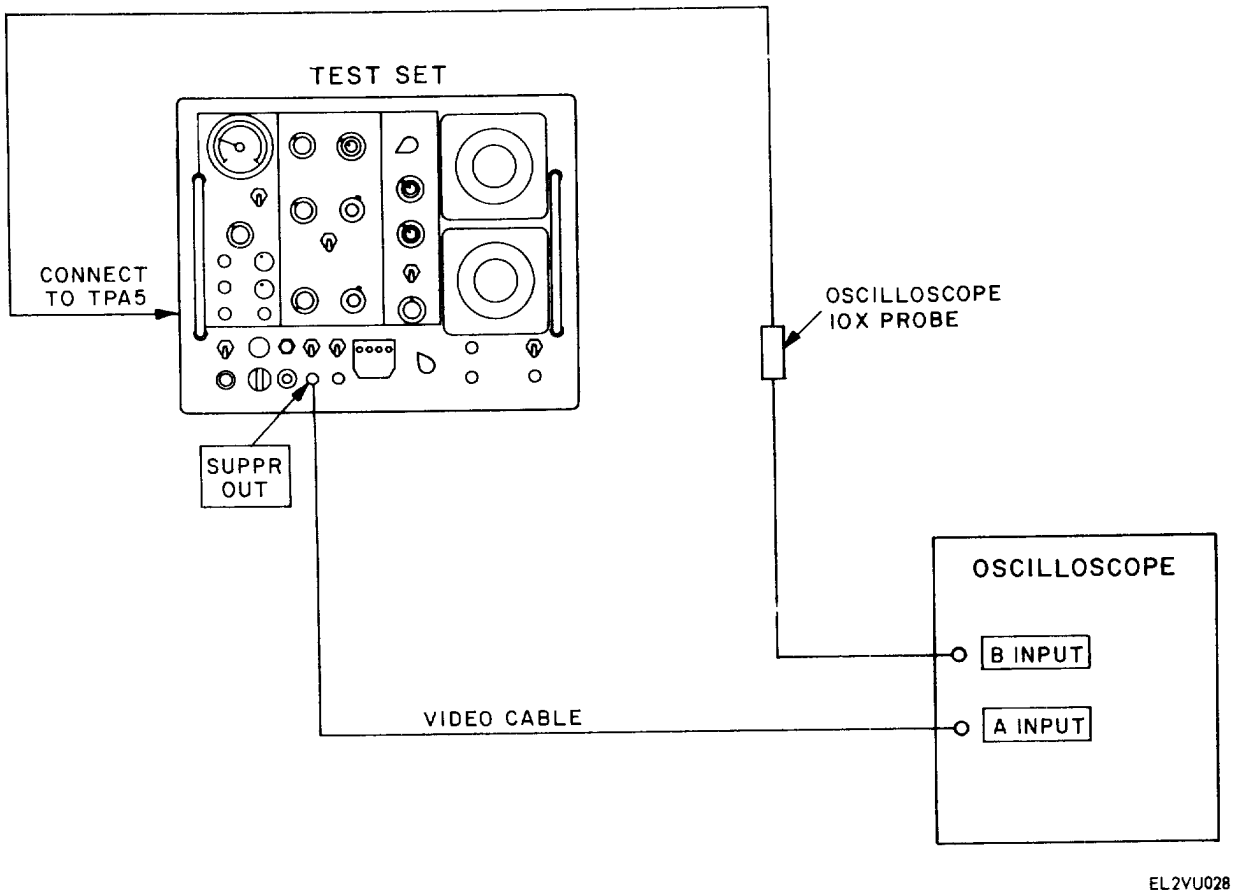


Figure 3-19. Suppression pulse test setup.

Table 3-12. Mode 4 Interface Input and Output Function Test Procedure

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	performance standard
1	Set up oscilloscope. Apply a positive pulse of 1.5 volts amplitude 0.5 μsec. duration with a pulse rate of 500 HZ and rise time of 0.05 μsec.	Set up test set per paragraph *3-4a.*	Connect test set up as shown in figure 3-20. Set oscilloscope DISPLAY switch to ALT Measure spacing between leading edges of pulse on B INPUT and 1st pulse on A INPUT.	Pulse spacing is 200 ± 5 μsec.
2			Measure pulse width of 1st pulse on A INPUT at 50% of pulse amplitude.	Pulse width is 0.5 ± 0.1 μsec.
3			Measure pulse amplitude	Pulse amplitude is 5.0 ± 0.5 volts,
4			Measure spacing between 1st and 2nd pulses leading edge to leading edge.	Pulse spacing is 1.8 ± 0.1 μsec.
5		CHAL INHIB switch ISLS ON	Observe pulses on A INPUT are inhibited.	Pulses are inhibited
6		CHAL INHIBIT switch activated to DISPARITY (MOM)	Observe pulses on A INPUT are inhibited.	Pulses are inhibited.

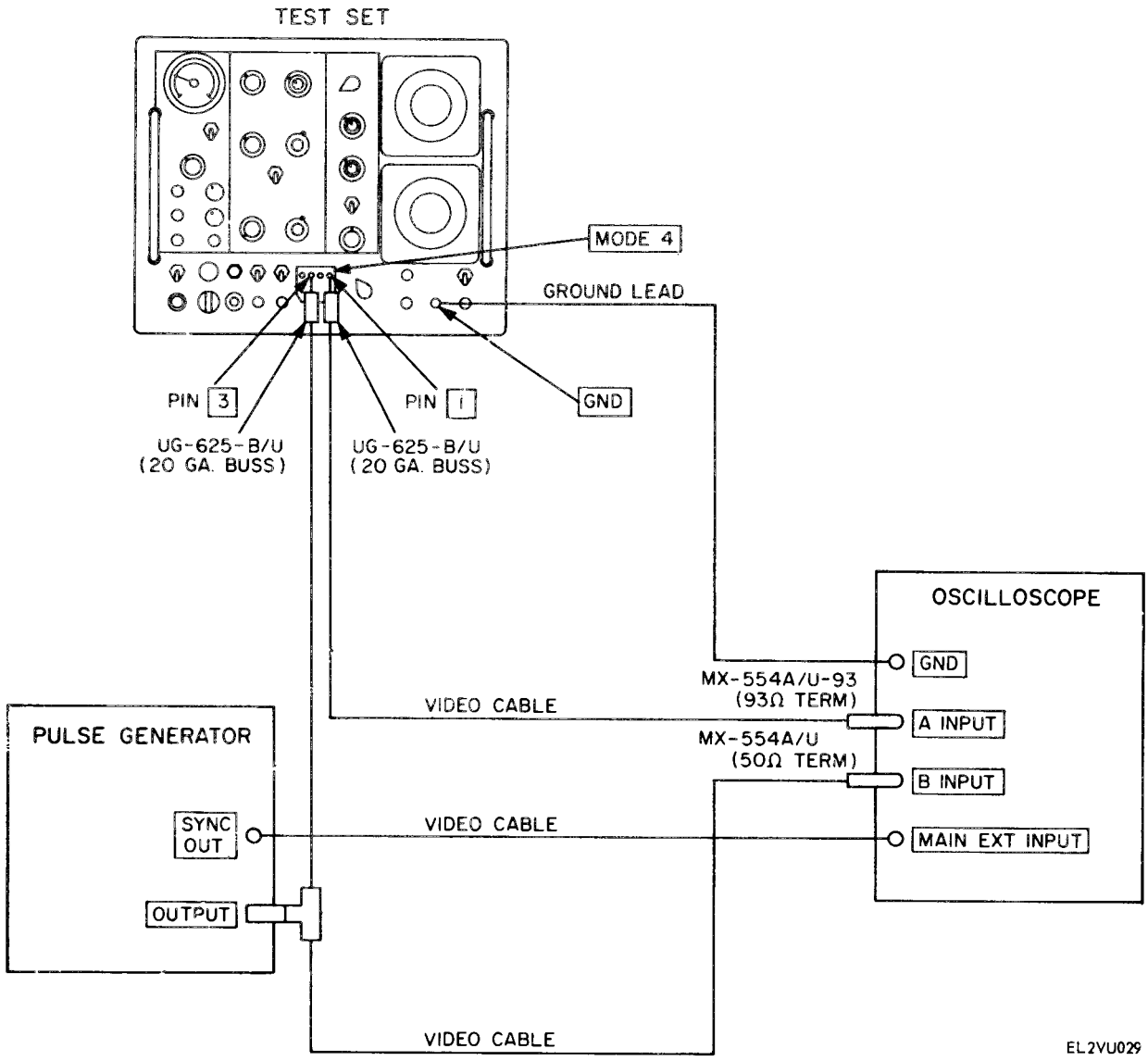


Figure 3-20. Mode 4 reply test setup.

Table 3-12. Mode 4 Interface Input and Output Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
7		CHAL INHIBIT switch OFF	Disconnect connector from pulse generator PULSE OUT jack.	Three pulses reply disappear from A INPUT.
8		CHAL MODE SELECT switch 4A PRF SELECT X-1/2	Press test set BIT (MOM) switch while observing A INPUT.	Three pulse reply is present.

Table 3–13. Mode 4 Disparity Function Test Procedure

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
1		Set up test set per paragraph *3-4a* CHAL WIDTH SELECT switch 0.50 CHAL MODE SELECT switch 4A. PRF SELECT X-1/2	Connect test set up as shown in figure 3-21 Observe Oscilloscope display.	Mode 4 challenge word is present on B INPUT.
2			Set and hold test set CHAL INHIB switch to DISPARITY (MOM) position; observe pulse in 66 μsec position (26th pulse) of the mode 4 challenge word.	Pulse in 66 μsec position 26th pulse is inhibited and transfers from B INPUT to A INPUT.
3		CHAL INHIBIT switch ISLS ON	Press hold BIT (MOM) switch. Adjust oscilloscope DIV DELAY control to center last pulse on B INPUT on CRT graticule. Measure spacing between last pulse on B INPUT and pulse on A INPUT.	Pulse on A INPUT is within ± 1 μsec of last pulse on B INPUT, leading edge to leading edge.
4			Measure amplitude of pulse on A INPUT while pressing BIT MOM switch.	Pulse amplitude is 5 ±0.5 volts.
5			Measure width of pulse on A INPUT while pressing BIT (MOM) switch.	Pulse width is 0.5 ± 0.1 μsec.

Table 3 - 14. SIF Reply Marker Function Test Procedure

Step No.	Control Settings: Test equipment	Control Settings: Test set	Test procedure	Performance standard
1		Set up test set per para graph *3-4a.*	Connect test setup as shown in figure 3-22. Observe that four markers occur on B INPUT starting 2 to 4 μsec. after 2nd pulse on A INPUT.	Four markers appear on B INPUT.
2			Adjust oscilloscope DIV DELAY control to view second pulse on *A* INPUT and first pulse on B INPUT. Vary MEASUREMENT MKR PHASING control throughout entire range and measure spacing between 2nd pulse on A lNPUT and 1st pulse on B INPUT	Pulse spacing can be varied from less than 2 μsec to more than 4 μsec.
3			Using oscilloscope DIV DELAY control locate 1st pulse on B INPUT Measure pulse amplitude.	Pulse amplitude is 0.5 volt min.

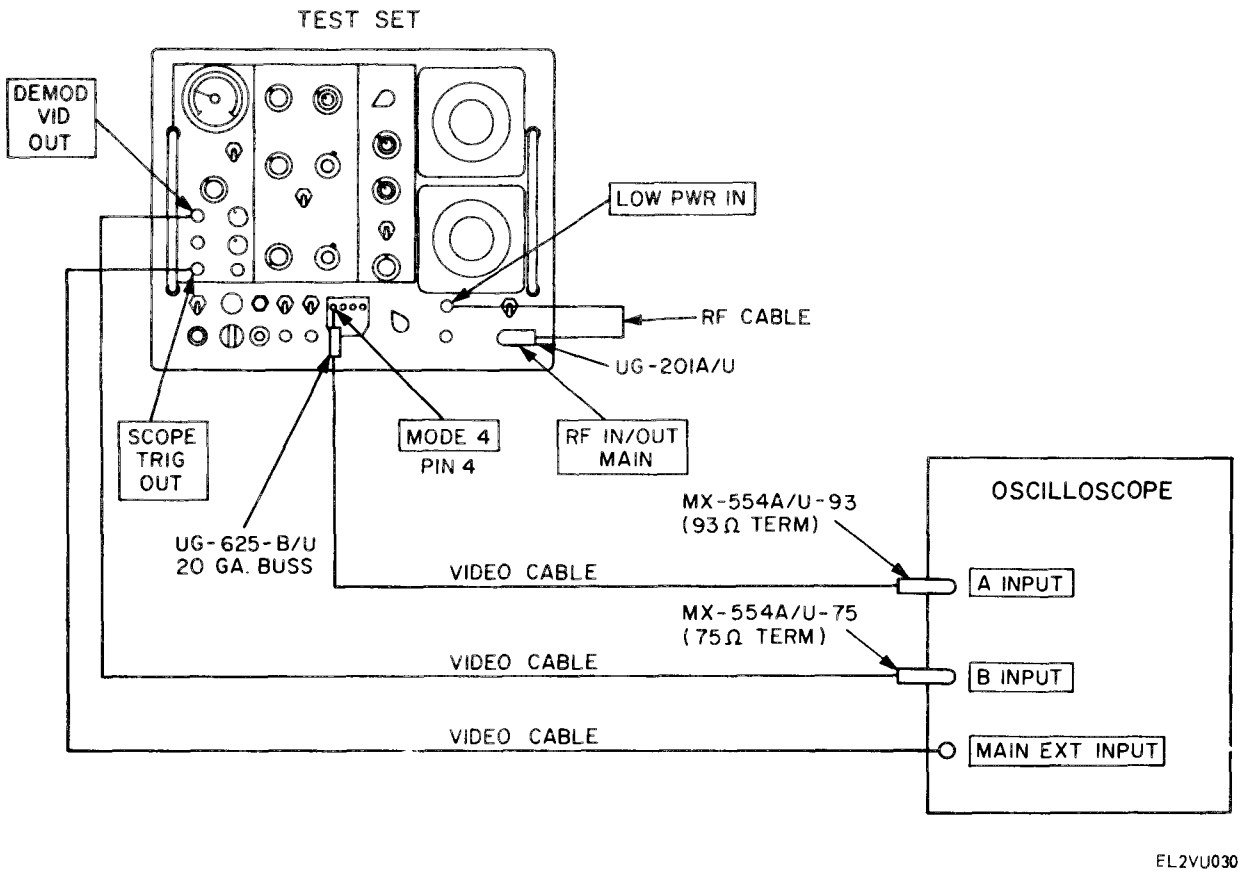


Figure 3-21. Mode 4 disparity test setup.

Table 3-14. SIF Reply Marker Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
4			Measure pulse width.	Pulse width is 0.15 ± 0.5 μsec.
5			Disconnect cable from test set DEMOD VID OUT jack. Connect cable to TIMING MRKS OUT jack to oscilloscope A INPUT jack.	Pulse spacing is 20.30 ± 0.02 μsec.
6			Measure spacing between 1st and 3rd pulses.	Pulse spacing is 24.65 ± 0.02 μsec.
7			Measure spacing between 1st and 4th pulses.	Pulse spacing is 49.30 ± 0.02 μsec.

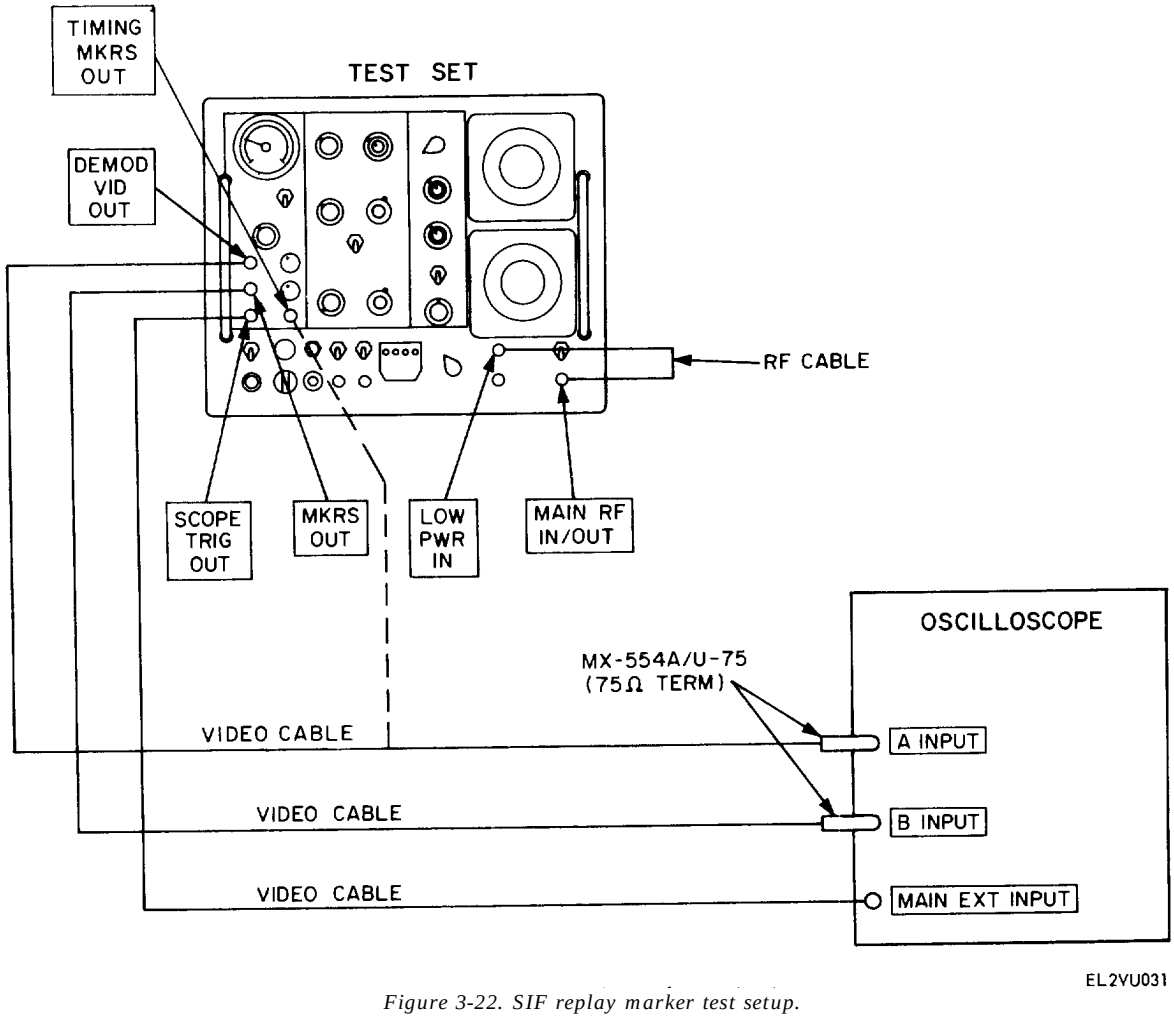


Figure 3-22. SIF replay marker test setup.

Table 3-15. RF Output Frequency Function Test Procedures

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3-23	Set up test set per paragraph *3-4a* and as follows: CHAL MODE SELECT switch CW		Frequency is 1030 ±0.1 MHz
2	Set oscilloscope DISPLAY switch to ALT	SIG GEN FCTN switch SWP ± 5 MHZ	Observe 1025 to 1035 MHz MARKERS ON B INPUT as shown in figure 2-5. Adjust frequency comparator FREQUENCY" MEGACYCLES control until zero beat on A INPUT is aligned with leading edge of 1st (1025 MHz) marker on B INPUT. NOTE When measuring any marker frequency, during final aligning set oscilloscope sweep	Frequency is 1025 ±0.1 MHz

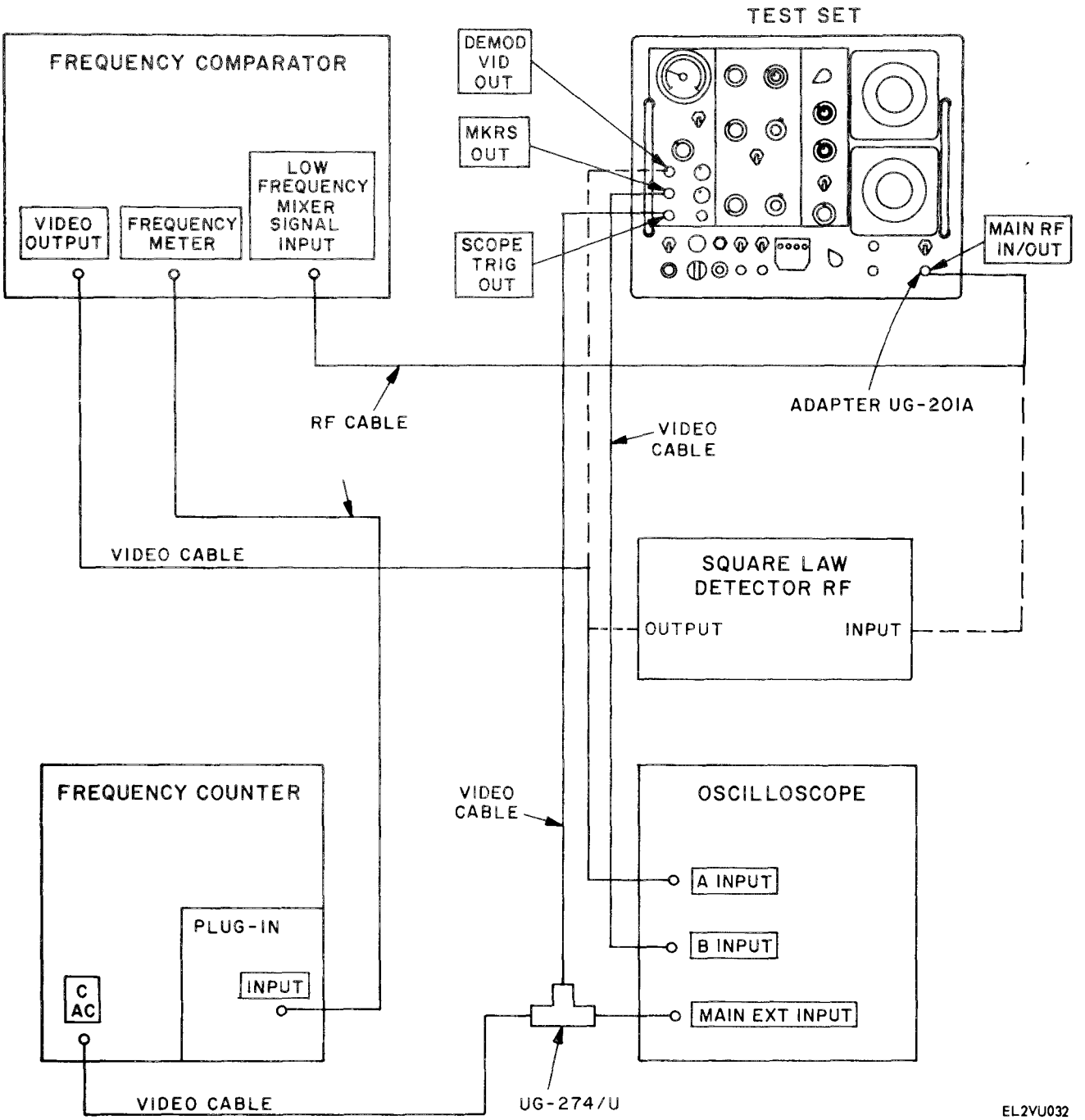


Figure 3-23. RF output frequency test setup.

Table 3–15. RF Output Frequency Function Test Procedure—Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
2 (Cont)			display switch to DELAYED. Adjust DIV DELAY control to view markers (as referenced by zero beat).	
3			Adjust frequency comparator FREQUENCY MEGACYCLES control until zero beat on A INPUT is aligned with leading edge of 2nd marker.	Frequency is 1027 ±0.1 MHz
4			Adjust frequency comparator FREQUENCY MEGACYCLES control until zero beat is aligned with leading edge of 3rd marker. Observe frequency counter indication.	Frequency is 1029 ±0.1 MHz
5			Adjust frequency comparator FREQUENCY MEGACYCLES control until zero beat is aligned with leading edge of 4th marker. Observe frequency counter indication.	Frequency is 1030 ±0.1 MHz
6			Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is aligned with leading edge of 5th marker. Oserve frequency counter indication.	Frequency is 1031 ±0.1 MHz
7			Adjust frequency comparator FREQUENCY MEGACYCLES control until zero beat is aligned with marker. Observe frequency counter indication.	Frequency is 1033 ±0.1 MHz
8			Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is aligned with leading edge of 7th marker. Observe frequency counter indication.	Frequency is 1035 ±0.1 MHz
9		SIG GEN FCTN switch ±20 MHz	Observe number of markers in one complete display Two additional markers shall appear. See Figure 2-5.	Display contains nine markers.
10			Adjust frequency comparator FREQUECNY MEGACYCLES controls until zero heat is aligned with leading edge of 1st marker. Observe frequency counter indication.	Frequency is 1010 ±0.3 MHz

Table 3-15. RF Output Frequency Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
		NOTE 2nd through 8th markers were checked previously.		
11			Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is aligned with leading edge of 9th marker. Observe frequency counter indication.	Frequency is 1050 ±0.3 MHz
12			Observe frequency counter indication.	Frequency is 225 to 275 Hz
13		Set SIG GEN FCTN switch to SWP ±5 MHZ	Observe frequency counter indication.	Frequency is 720 to 880 Hz
14		Set CHAL MODE SELECT switch to 1. MEASUREMENT FUNCTION SELECT switch to FREQ	Disconnect cable from comparator VIDEO OUTPUT and connect to test set DEMOD VIDEO OUT. Depressing test set BIT (MOM) switch. Using the markers displayed on B INPUT, determine BIT oscillator frequency.	Frequency is 1090 ±0.3 MHz. For final measurement set oscilloscope sweep display switch to DELAYED and adjust DIV DELAY control to view 1089, 1090, and 1091 MHz markers.

Table 3-16. RF Power Output Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test equipment as shown in figure 3-24.	Set up test set per paragraph 3-4*a* except as follows: CHAL MODE SELECT switch to CW.	Using rf power meter determine rf output power.	-10 ±1.0 dBm
2		MAIN ATTEN control to -15 dBm	Determine rf output power.	-15 ±1.0 dBm
3		MAIN ATTEN control to -20 dBm	Determine rf output power.	-20 ±1.0 dBm
4			Disconnect cable from test set set RF IN/OUT MAIN jack and connect to AUX jack. Determine rf output power.	-10 ±1.0 dBm
5		AUX ATTEN control to -15 dBm	Determine rf output power.	-15 ±1.0 dBm
6		AUX ATTEN control to -20 dBm	Determine rf output power.	-20 ±1.0 dBm
7	Set up rf power meter to read power in the range of 0 dBm	AUX ATTEN control to -10 dBm. MAIN ATTEN control to -10 dBm.	Disconnect power meter from test set RF IN/OUT AUX jack. Disconnect test set W6-P1 from AT 3-J1 and W8-P1 from AT 4-J1. Connect power meter to W6-P1 through a reference rf cable. Cable to be used	

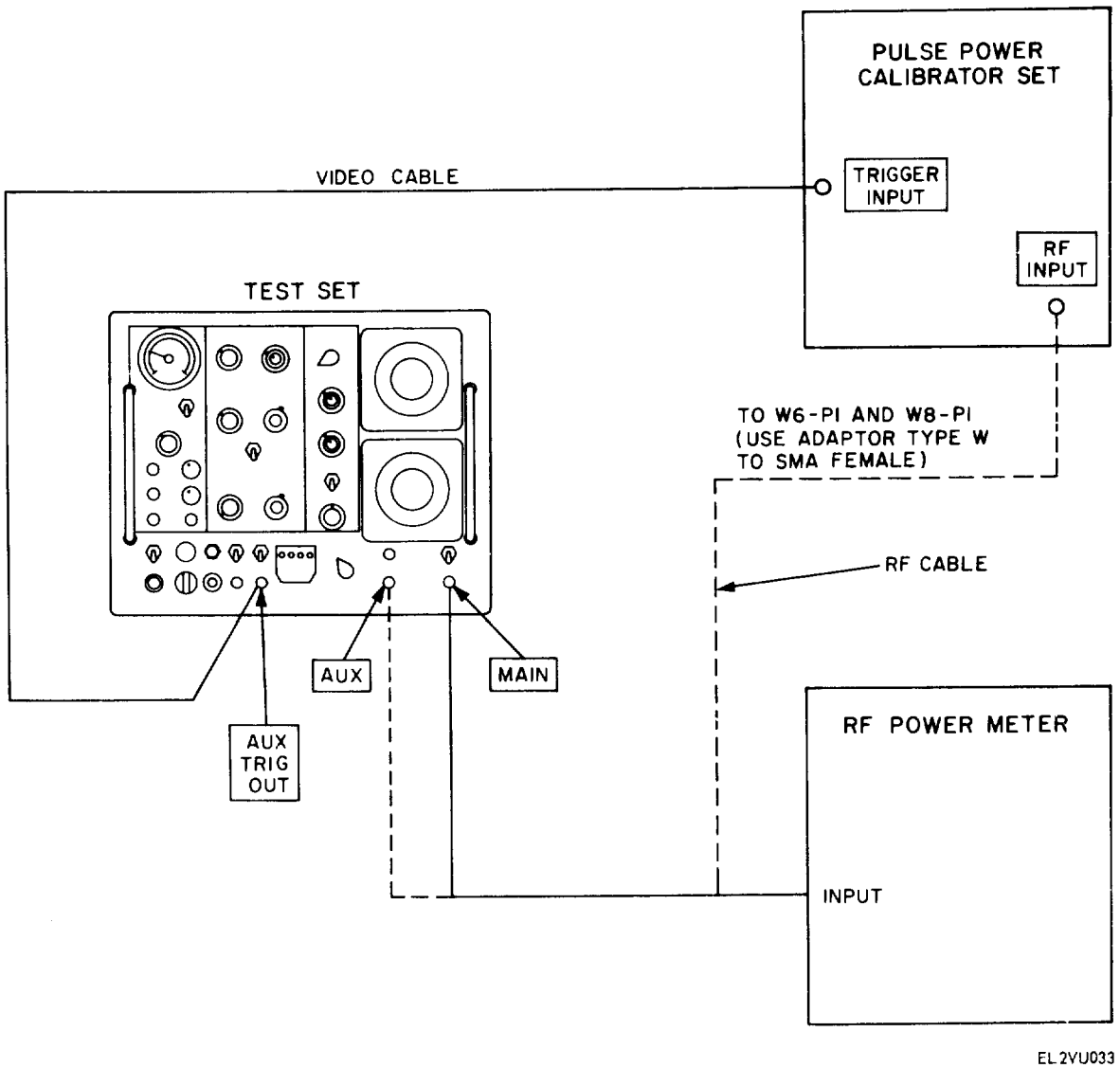


Figure 3-24. Rf power test setup.

Table 3-16. RF Power Output Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
7 (Cont)			later to connect to pulse power calibrator set input. Determine and note rf output power.	
8			Disconnect rf cable from test set W6-P1 and connect to W8-P1. Determine and note rf power output.	
9		Set CHAL MODE SELECT to C. Set CHAL WIDTH SELECT to VARY and fully cw. Set PRF select RANGE switch to X100.	Disconnect rf cable from power meter and test set cable W8-P1. Connect same rf cable from pulse power calibrator set R.F. INPUT to test set W6-P1.	
			Obtain difference between level indicated on pulse power calibrator set +DB, -DB window as corrected and level of step 7. This is cw to pulse difference for MAIN channel.	Level difference 1.0 dB max.
10			Disconnect rf cable from test set W6-P1 and connect to W8-P1.	
11			Obtain difference between level indicated on pulse power calibrator set +DB -DB window as corrected and rf power level in step 8. This is difference for AUX channel.	Level difference 1.0 dB max.
12			Disconnect rf cable from test set W8-P1. Connect W6-P1 to AT3-J1 and W8-P1 to AT4-J1.	

Table 3-17. Modulator and Demodulator Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1		Set up test set per paragraph 3-4*a*.	Connect test set up as shown in figure 3-25. Observe that two pulses are present. Adjust oscilloscope DIV DELAY control to position intensified trace over 2nd pulse.	
2			Using 0.1 μsec markers (B Channel) measure and record pulse width at 50% amplitude points.	Pulse width is 0.80 ± 0.05 μsec.

Table 3–17. Modulator and Demodulator Function Test Procedure—Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
3			Measure pulse rise time at the 1% and 81% amplitude points. Multiply the distance in divisions between the two points by the setting of the DELAYED TIME/DIV switch to obtain the rise time. Record result.	Pulse rise time is 0.05 to 0.10 μsec.
4			Using the procedure outlined in step 3 measure and record pulse fall time.	Pulse fall time is 0.05 to 0.20 μsec.
5		MEASUREMENT FUNCTION SELECT switch PRF CHAL	Disconnect square law detector from test set RF IN/OUT MAIN jack and oscilloscope A INPUT jack. Connect video cable from RF IN/OUT MAIN jack to LOW PWR IN jack and connect test set DEMOD VID OUT jack to oscilloscope A INPUT jack (with 75 obm termination).	
			Measure puke width	Puke width is within ± 0.02 μsec of width recorded in step 2.

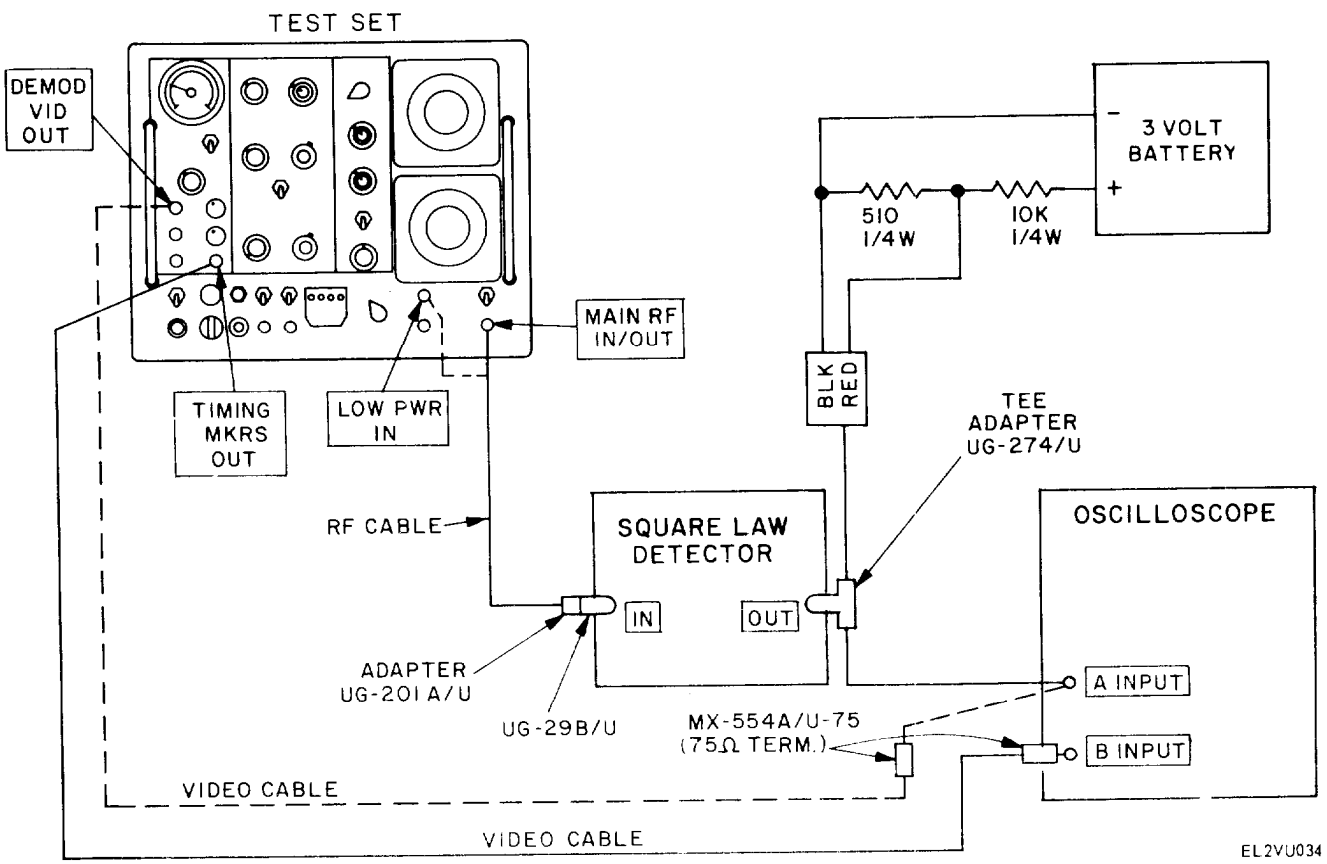


Figure 3–25. Modulator and demodulator test setup.

Table 3-17. Modulator and Demodulator Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
6			Adjust oscilloscope A INPUT VOLTS/DIV vernier control for a pulse amplitude of 8 divisions. Using oscilloscope CRT graticule, measure distance in divisions between 10% and 90% amplitude points on rising and falling edges.	Pulse rise and fall times are within 0.02 μsec of times recorded in steps 3 and 4.
7			Disconnect cable and termination from oscilloscope A INPUT jack. Connect square law detector between test set RF IN/OUT AUX jack and oscilloscope A INPUT jack and repeat steps 1 through 4.	Same as steps 1 thru 4

Table 3-18. Input Power Measurement Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3-26. Setup signal generator as follows: SIGNAL FREQUENCY control 1090 MEGACYCLES. O=DBM. Function switch RF. TRANSPONDER SET CONTROL MASTER switch LOW	Setup per paragraph 3-4a and as follows: MEASUREMENT FUNCTION SELECT switch PWR.	a. Set RF SELECTOR switch to MEASURE and TRIGGER NO.1 ON/OFF to ON. Note reading. b. Obtain reading from the +DB window. Using the ATTENUATOR CORRECTION CURVE in the Book of Charts, determine and note the corrected attenuator setting for 1090 MC. **NOTE** This setting is the reference power output level in dBm of the receiver-transmitters. c. Disconnect cable from pulse power calibrator set R.F. INPUT jack and connect to the test set RF IN/OUT MAIN jack.	

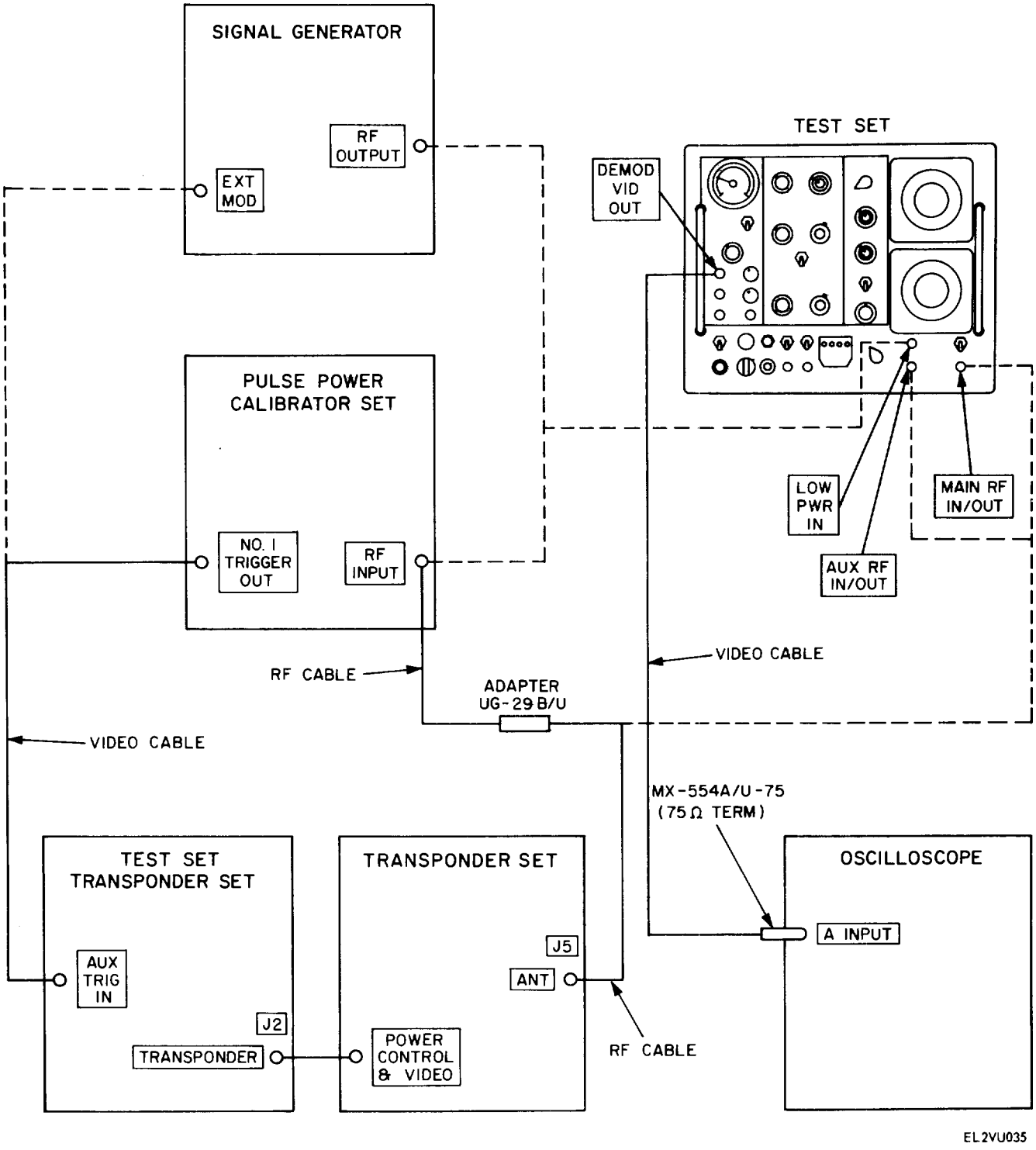


Figure 3-26. Input power test setup.

Table 3-18. Input Power Measurement Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
			d. Adjust test set MEASUREMENT DEMOD VIDEO LEVEL control until pulse on the oscilloscope display is 1.0 volt and note power indication on the test set MEASUREMENT meter. Determine and note the corresponding level in dBm for the reading obtained. e. Using subtraction, determine the level difference between the test set reading obtained in step *a*, and receiver/transmitter reading obtained in step *b*.	
2		RF IN/OUT DEMOD switch AUX	Disconnect cable from the test set RF IN/OUT MAIN jack and connect to AUX jack. Repeat steps 1*d* thru 1*e*. Perform complete procedure described in paragraph 3-10-1, and make indications adjustments only if results obtained in steps listed below does not meet performance standards given. *Paragraph 3-10-1 Step* — *Performance Standard* (h) — 17 to 19 dBW (k) — 32 to 34 dBW	The difference is 1.0 dB max.

Table 3-19. Frequency Measurement Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1	Connect test setup as shown in figure 3-27.	Set up test set per paragraph 3-4*a* and indicated below. SIG GEN FCTN switch SWP ±20 MHZ MEASUREMENT FUNCTION SELECT switch FREQ	a. Adjust signal generator frequency until maximum amplitude point of passband displayed on A INPUT is aligned with first marker on B INPUT. b. Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is indicated on frequency comparator display. (Adjust frequency comparator GAIN control as required to limit vertical amplitude of display). Adjust DIV DELAY control to view marker (as referenced by zero beat).	

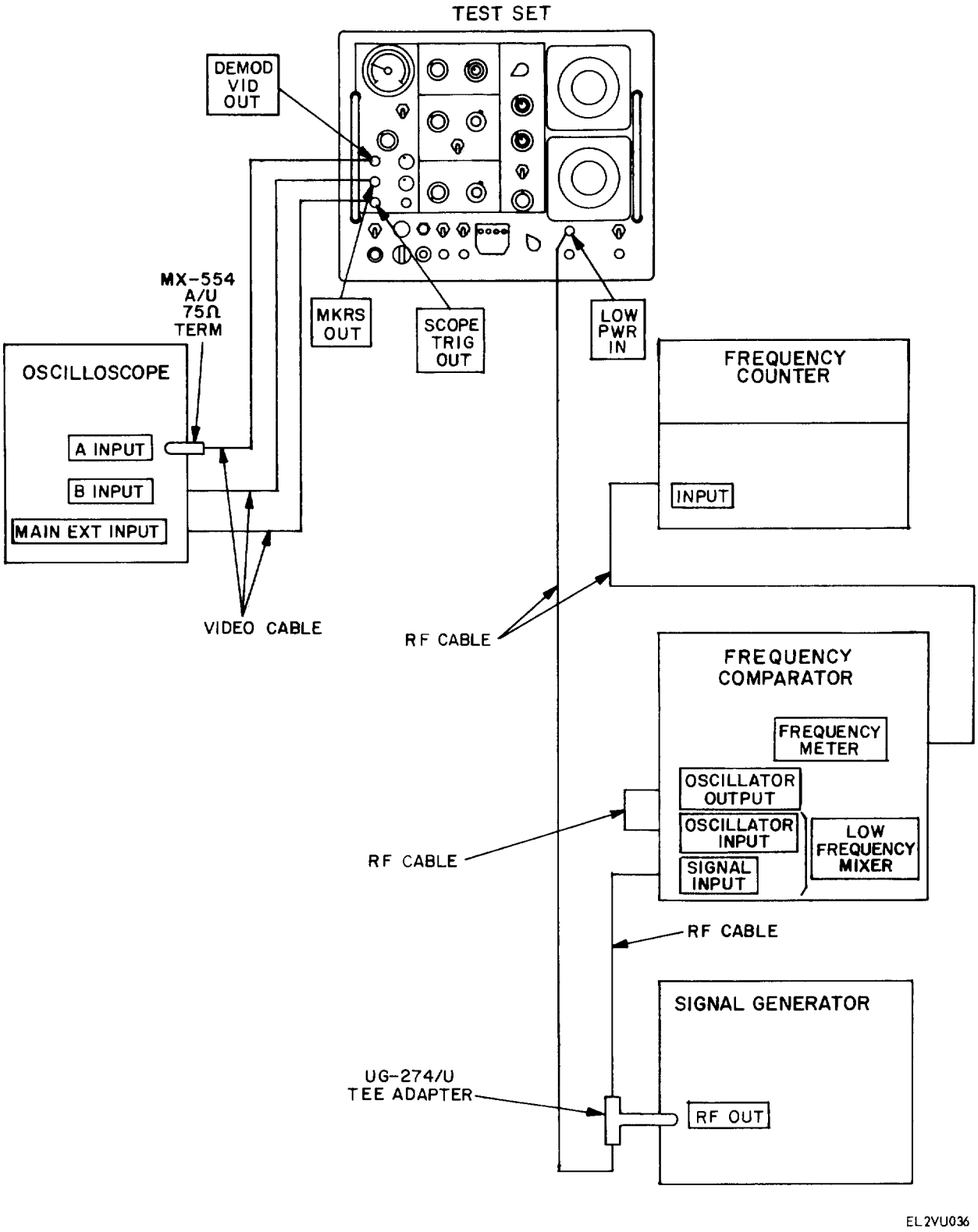


Figure 3–27. Frequency measurement test setup.

Table 3-19. Frequency Mesurement Function Test Procedure- Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (Cont)	Set signal generator to 1085 MHz and for an output level of 0 dBm.		c. Observe frequency counter indication.	Frequency is 1070 ± 0.6 MHz.
2			Adjust signal generator frequency until maximum points of the displayed pass band on A INPUT is centered in 2nd marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is indicated on frequency comparator display. Observe frequency counter indication.	Frequency is 1085 ± 0.2 MHz.
3			Adjust signal generator frequency until maximum point of displayed passband on A INPUT is centered in 3rd marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat indicated on frequency comparator display. Observe frequency counter indication.	Frequency is 1087 ± 0.2 MHz
4			Adjust signal generator frequency until maximum point of displayed passband on A INPUT is centered in 4th marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is indicated on frequency comparator display. Observe frequency counter indication.	Frequency is 1089 ± 0.2 MHz.
5			Adjust signal generator frequency until maximum point of displayed passband on A INPUT is centered in 5th marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is indicated on frequency comparator display. Observe frequency counter indication.	Frequency is 1090 ± 0.2 MHz.
6			Adjust signal generator frequency until maximum point of displayed passband on A INPUT is centered in 6th marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero	Frequency is 1091 ± 0.2 MHz.

Table 3-19. Frequency Measurement Function Test Procedure—Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
6 (Cont)			beat is indicated on frequency comparator display. Observe frequency counter indication,	
7			Adjust signal marker frequency until maximum point of displayed passband on A INPUT is centered in 7th marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until zero beat is indicated on frequency comparator display. Observe frequency counter indication.	Frequency is 1093 ± 0.2 MHz.
8			Adjust signal generator frequency until maximum point of displayed passband on A INPUT is centered in 8th marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until a zero beat is indicated on frequency comparator displayed. Observe frequency counter indication.	Frequency is 1095 ± 0.2 MHz,
9			Adjust signal generator frequency until maximum points of displayed passband on A INPUT is centered in 9th marker on B INPUT. Adjust frequency comparator FREQUENCY MEGACYCLES controls until a zero beat is indicated on frequency comparator display. Observe frequency counter indication,	Frequency is 1110 ± 6 MHz

Table 3-20. Timing Marker Function Test Procedure

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1		Set up test set per paragraph *3-4a.*	Connect test setup as shown in figure 3-28; observe three sets of pulses. Each set will be of different amplitude and spacing.	Three sets of pulses are present. Pulse amplitude ≥ 0.5 volts.
			a. Measure spacing from leading edge to leading edge of Higher Amplitude set of pulses.	Pulses are spaced 10.0 µsec ± 0.2% Pulse amplitude is ≥ 0.5 volts.
			b. Measure spacing and amplitude of second set of pulses. (Amplitude is less than previous pulses hut Greater than smallest.)	Pulses are spaced 1.0 µsec. Pulse amplitude is ³ 0.5 volts.

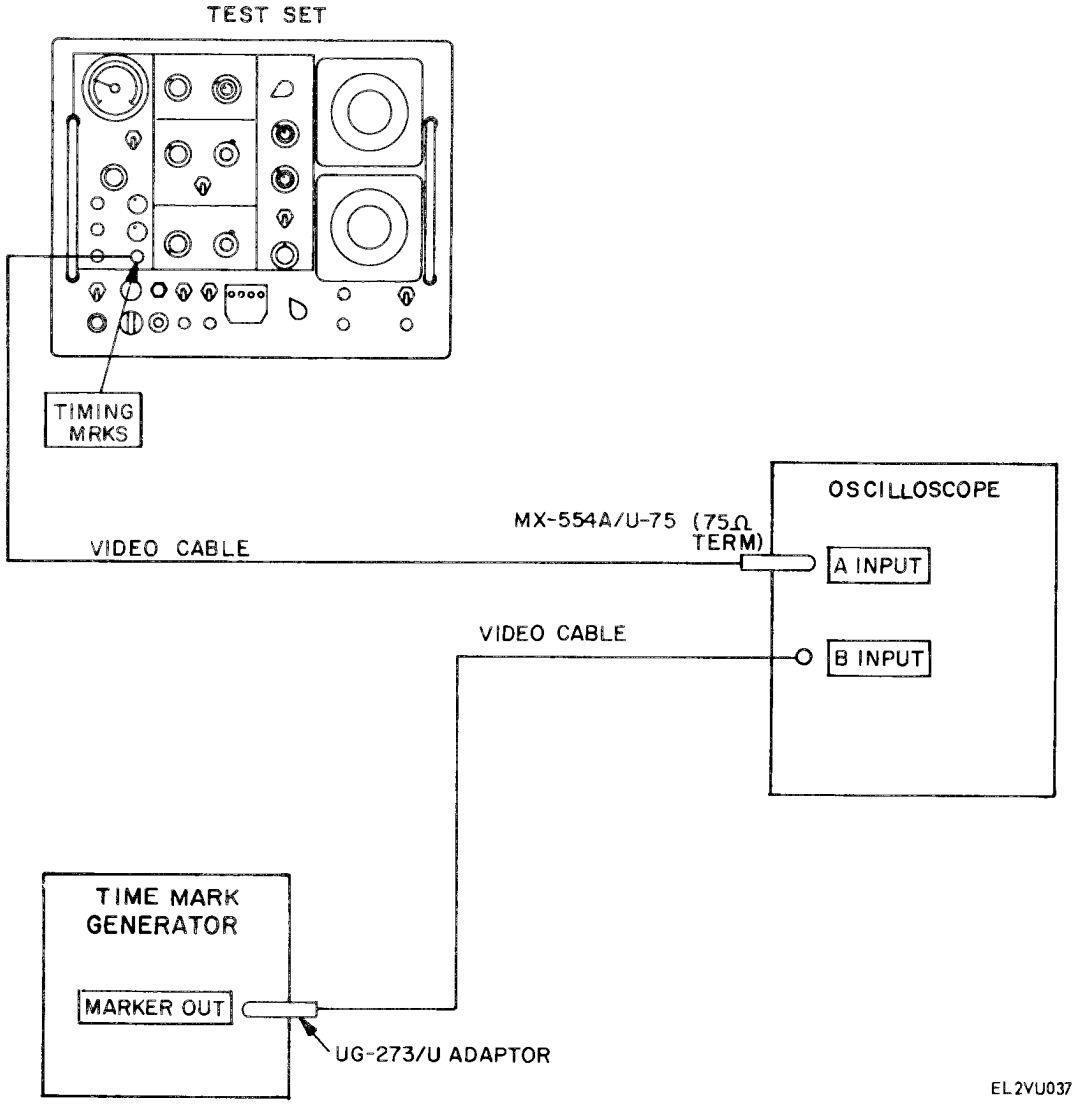


Figure 3-28. Timing marker test setup.

Table 3-20. Timing Marker Function Test Procedure - Continued

Step No.	Control Settings		Test procedure	Performance standard
	Test equipment	Test set		
1 (Cont)	Set up time mark generator as follows: Apply a 1.0 μsec signal.		c. Observe third set of pulses. (This set of pulses are the smallest of the three sets).	Pulses are spaced 0.1 μsec from leading edge to leading edge. Pulse amplitude is ≥ 0.5 volts.

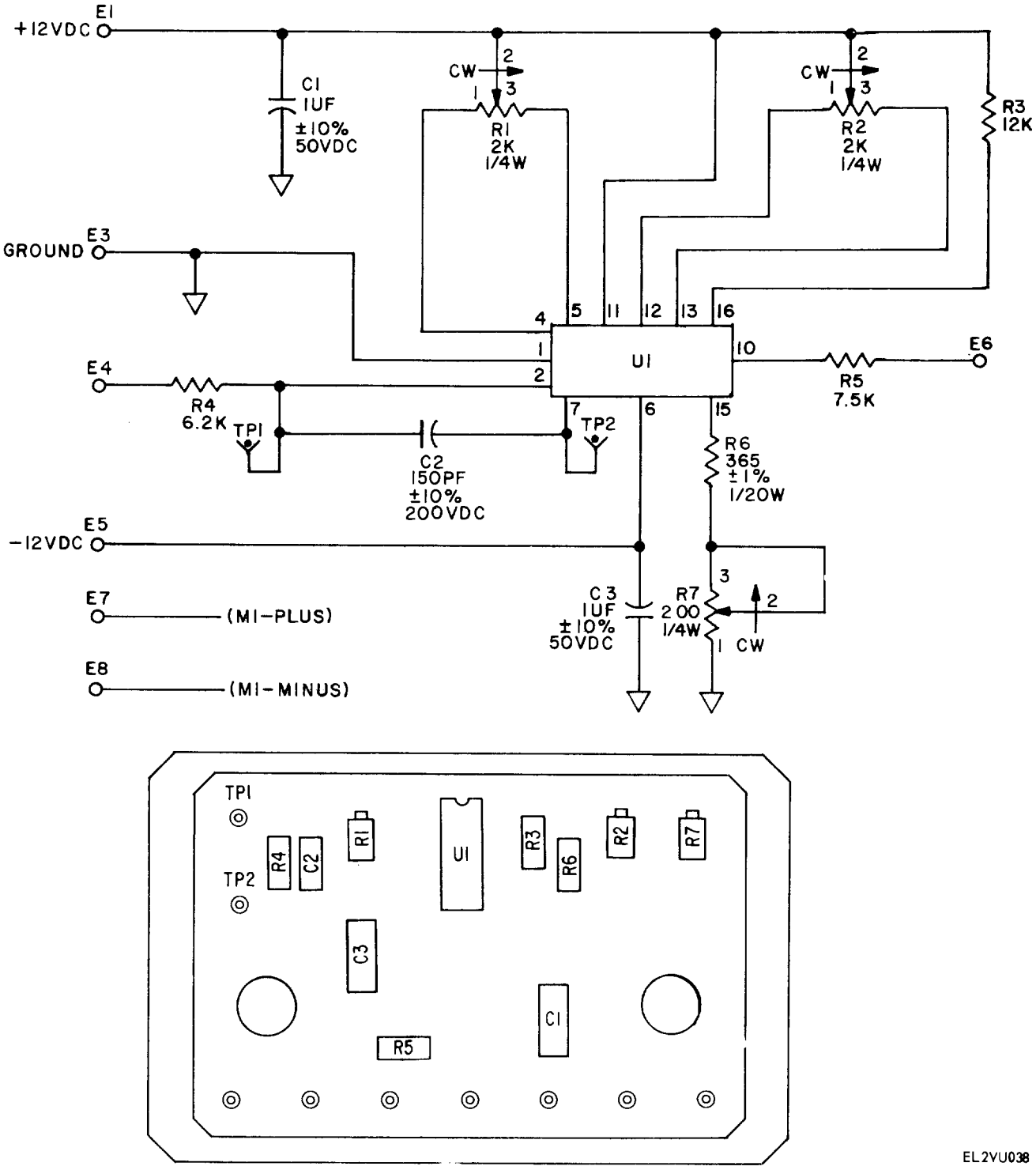


Figure 3–29. Meter circuit board M1A1 schematic and parts location diagram.

APPENDIX

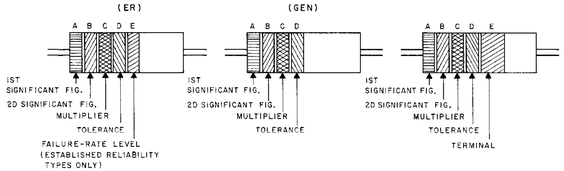
REFERENCES

The following is a list of publications available for General Support Maintenance of Test Set, Transponder set AN/APM-305A.

DA Pam 310-4	Index of Technical Publications: Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA Pam 310-7	US Army Equipment Index of Modification Work Order.
TM 11-5895-490-20	Oranizational, Maintenance Manual Receiver-transmitters, Radio RT-859/APX-72 and RT-859A/APX-72 and Mountings, MT-3809/APX-72 and MT-3948/APX-72.
TM 11-6625-200-15	Operator's Organizational, DS, GS and Depot Maintenance Manual Multimeters ME-26A/U, ME26B/U, ME-26C/U, and ME-26D/U.
TM 11-6625-368-10	Operators Manual Pulse Generator Sets AN/UPM-15 and AN/UPM-15A.
TM 11-6625-402-15	Operator, Organizational, Field and Depot Maintenance Manual Pulse Power Calibrator Set AN/UPM-73.
TM 11-6625-493-15	Operator's, Organizational, DS, GS, and Depot Maintenance Manual Frequency Comparator CM-77A/USM.
TM 11-6625-1549-15	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual: Test Set, radio frequency power AN/USM-260 (NSN 6625-00-917-3099).
TM 11-6625-537-14-1	Operator's, organizational, Direct Support, and General Support Maintenance Manual Electronic Voltmeters ME-202A/U (NSN 6625-00-709-0288) and ME-202B/U (NSN 6625-00-972-4046).
TM 11-6625-542-15	Operator, organizational, Field and Depot Maintenance Manual Electronic Marker Generator AN/USM-108.
TM 11-6625-700-10	Operator's Manual Digital Readout, Electronic Counter AN/USM-207. (NSN 6625-00-911-6368)
TM 11-6625-842-15	Operation and Service/Organizational, GS and Depot Maintenance Manual with Illustrated Parts Breakdown Test Set, Transponder Set AN/APM-239A.
TM 11-6625-1517-15	Organizational, DS, GS, and Depot Maintenance Manual Signal Generator (Hewlett Packard HP 8614A) (AN/USM-213).
TM 11-6625-1703-15	Operator's, Organizational, DS, GS, and Depot Maintenance Manual Oscilloscope AN/USM-281A (NSN 6625-00-228-2201).
TM 38-750	The Army Maintenance Management System (TAMMS)

INDEX

U.S. GOVERNMENT PRINTING OFFICE : 1992 - 311-831 (44035)



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR-CODE MARKING FOR FILM TYPE RESISTORS

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS) ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL

RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

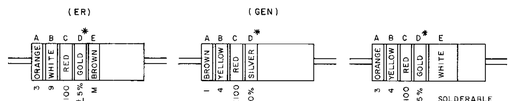
FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

TABLE 1
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

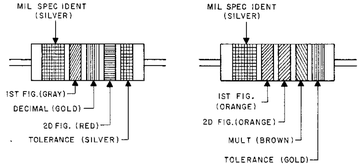
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD



(A) 8.2UH ± 10%

(B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED.

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN		10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

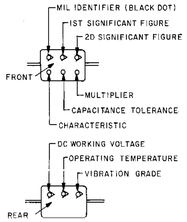
B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS

EL2V1039

FIG-10 Color code for military standard resistors, inductors, and capacitors (sheet 1 of 2).

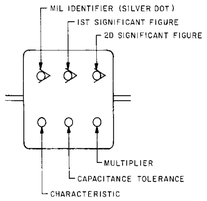
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM,CN,CY, AND CB.

CM



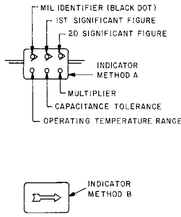
MICA-DIELECTRIC

CN



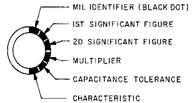
PAPER-DIELECTRIC

CY

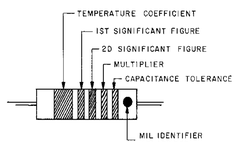


GLASS-DIELECTRIC, GLASS CASE

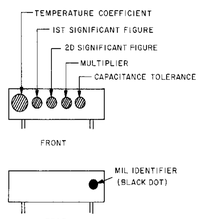
CB



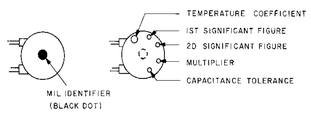
MICA, BUTTON TYPE



AXIAL LEAD



RADIAL LEAD



DISK-TYPE

TABLE 3- FOR USE WITH STYLES CM,CN,CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY,CM	CM
BLACK	CM,CY CB	0	0	1			±20%	±20%		A			-55°C TO +70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°C TO +85°C	
ORANGE		3	3	1,000		30%			D		D	300		
YELLOW		4	4	10,000					E				-55°C TO +125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°C TO +150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4- TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

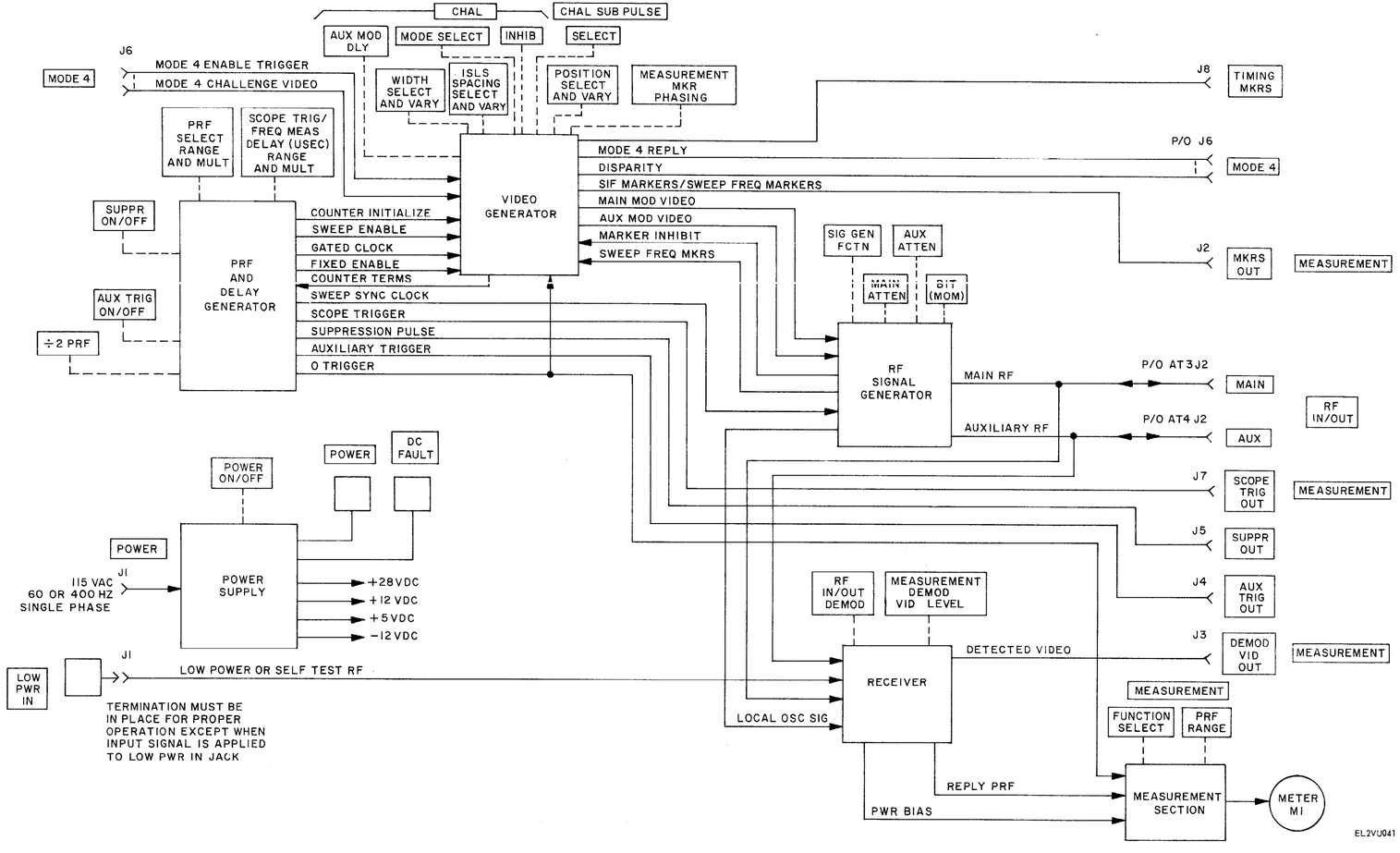
1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

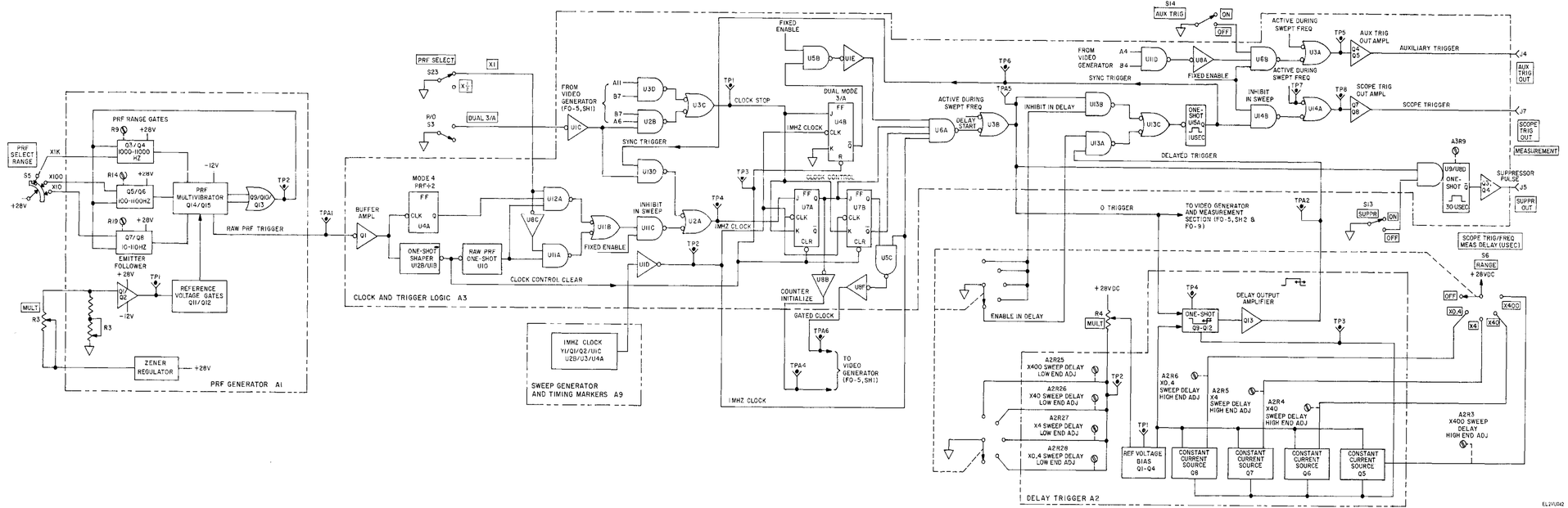
C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

EL2VUG40

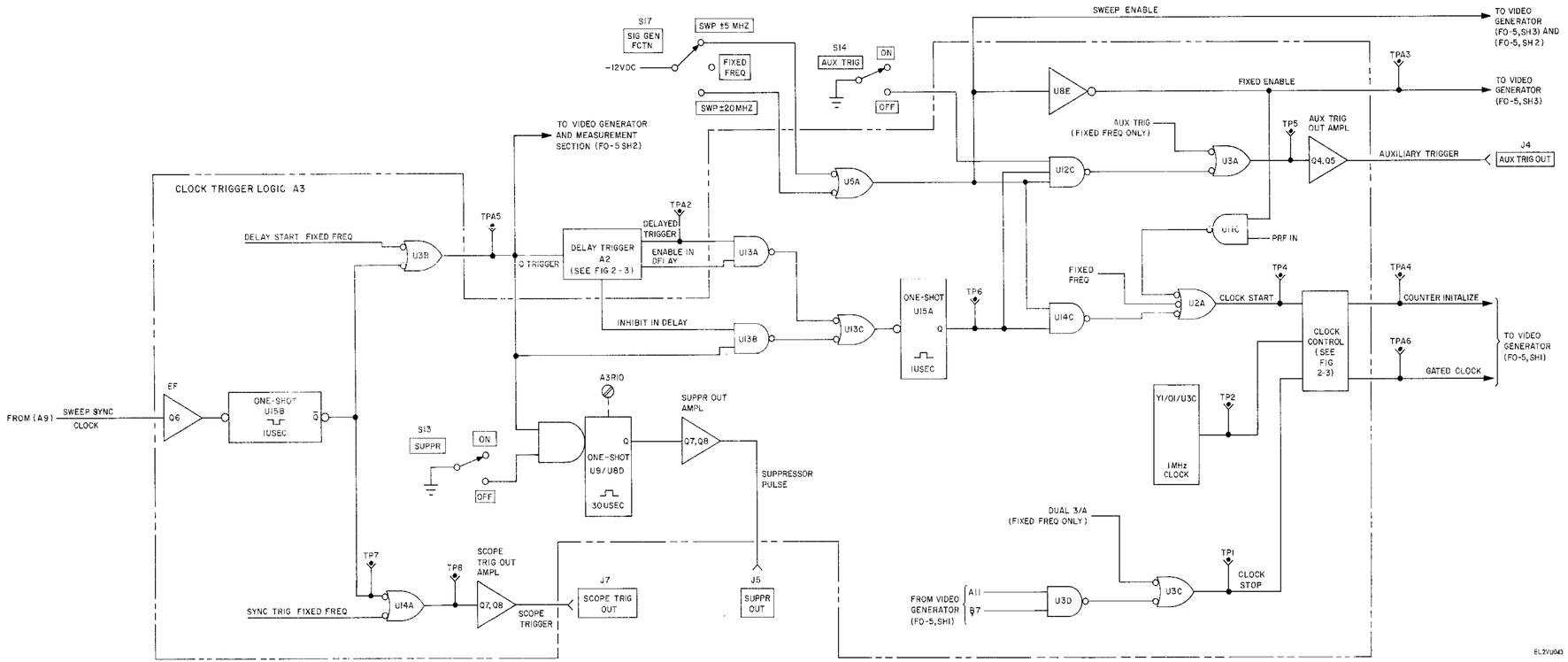
FG-1© Color code for military standard resistors, inductors, and capacitors (sheet 2 of 2).



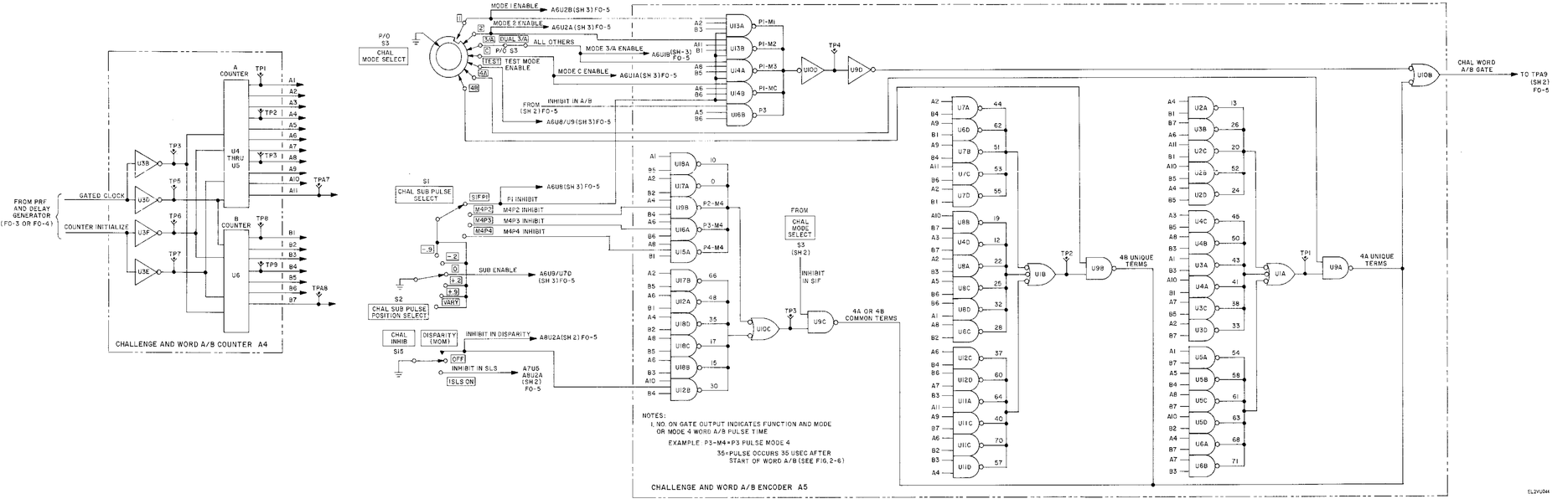
FO-2 *Test set block diagram.*



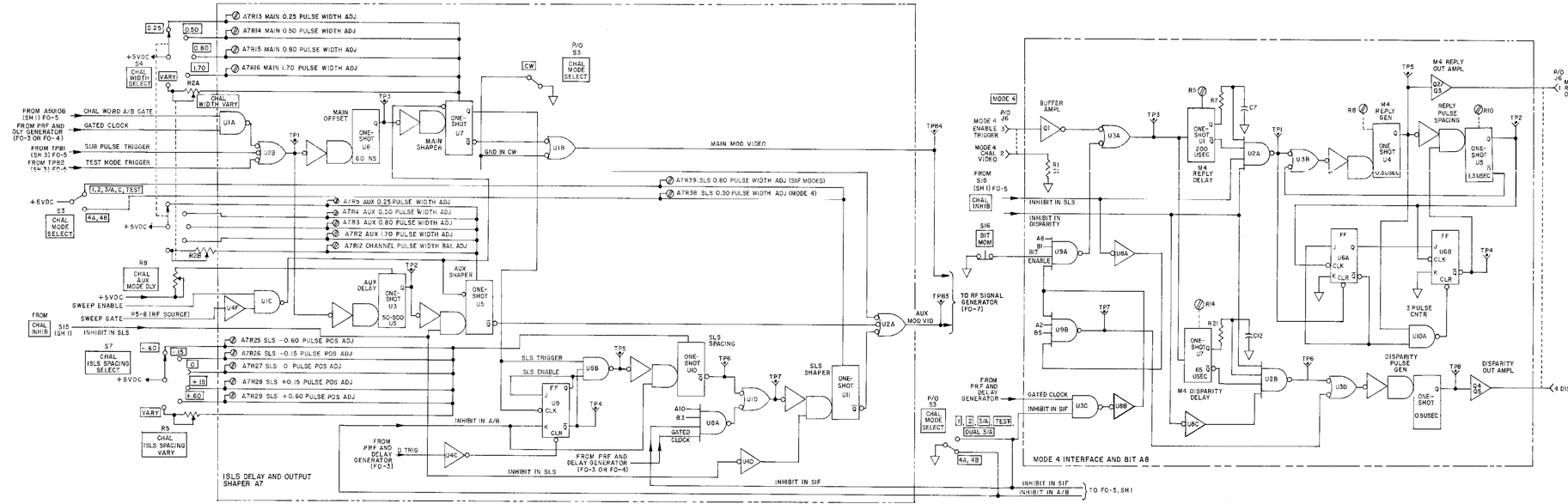
FO-5 Prf and delay generator, fixed frequency operation logic diagram.



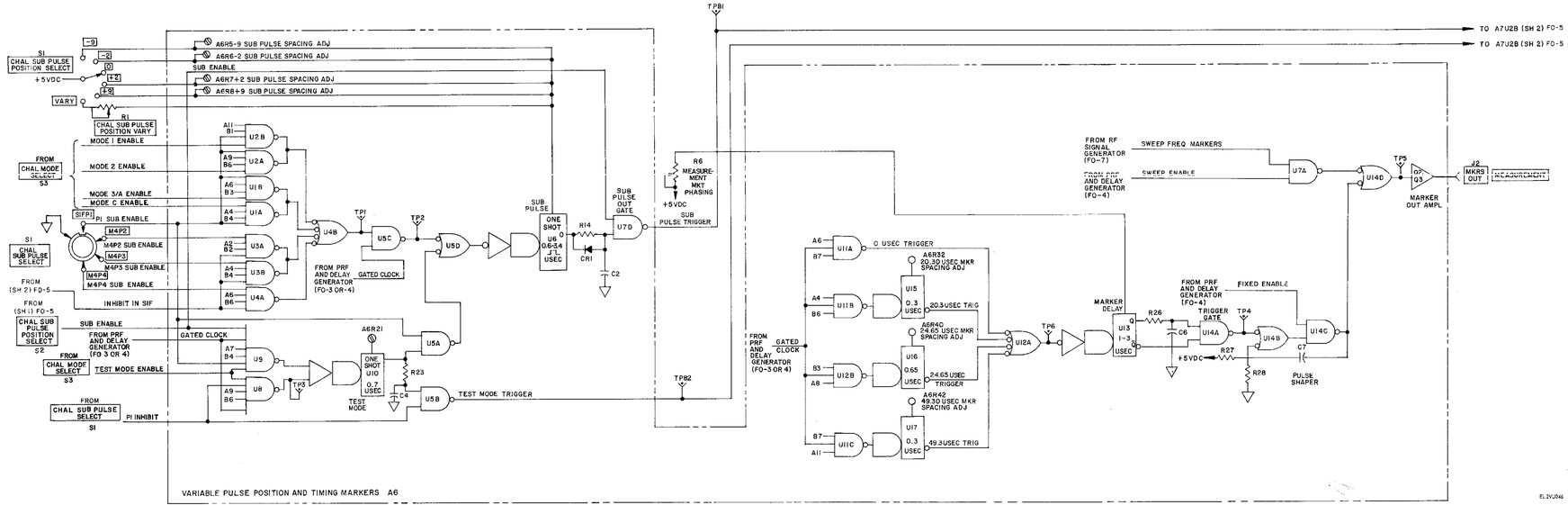
FO-4 Prf and delay generator, swept frequency operation logic diagram.



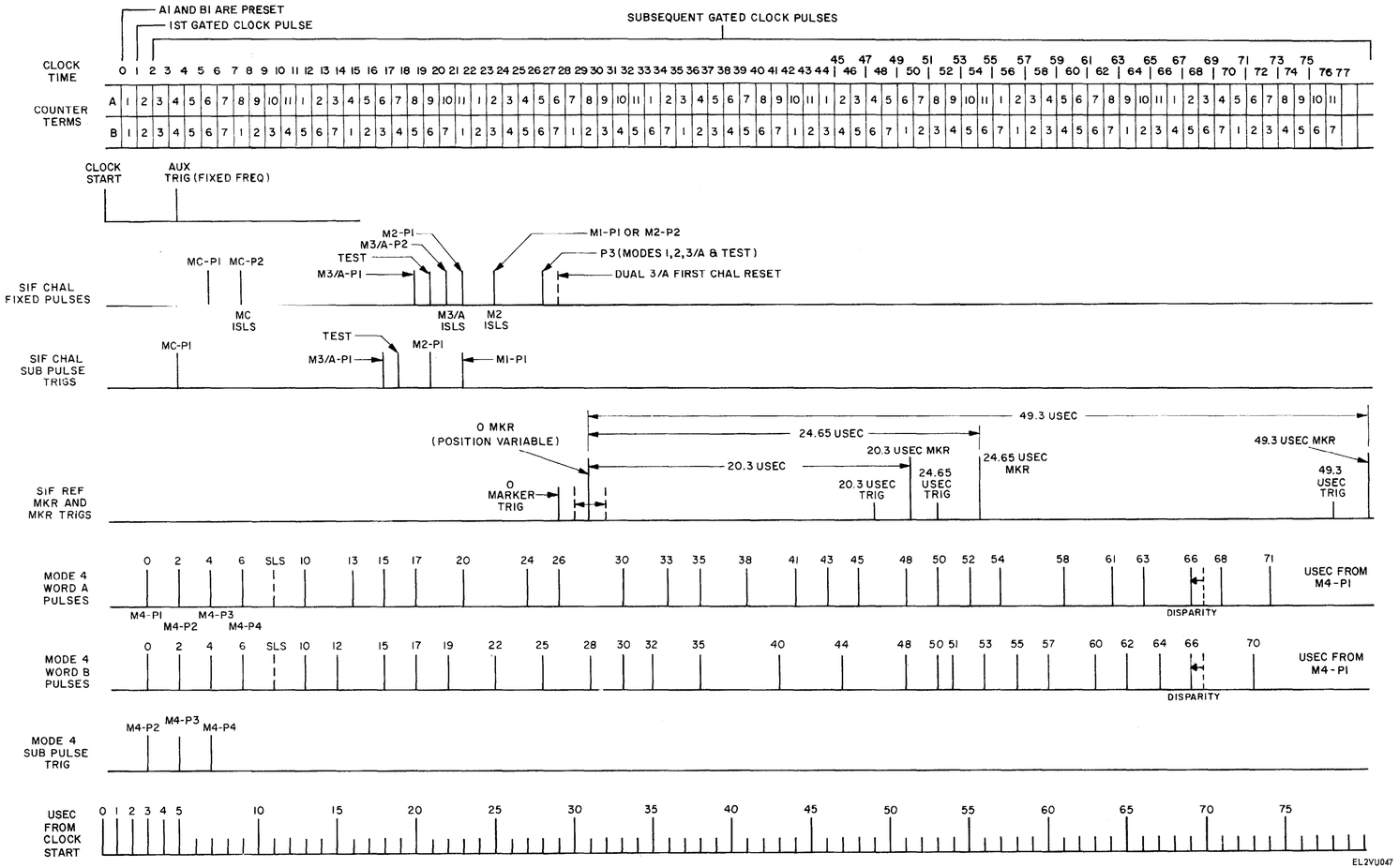
FO-10 Video generator logic diagram (sheet 1 of 4).



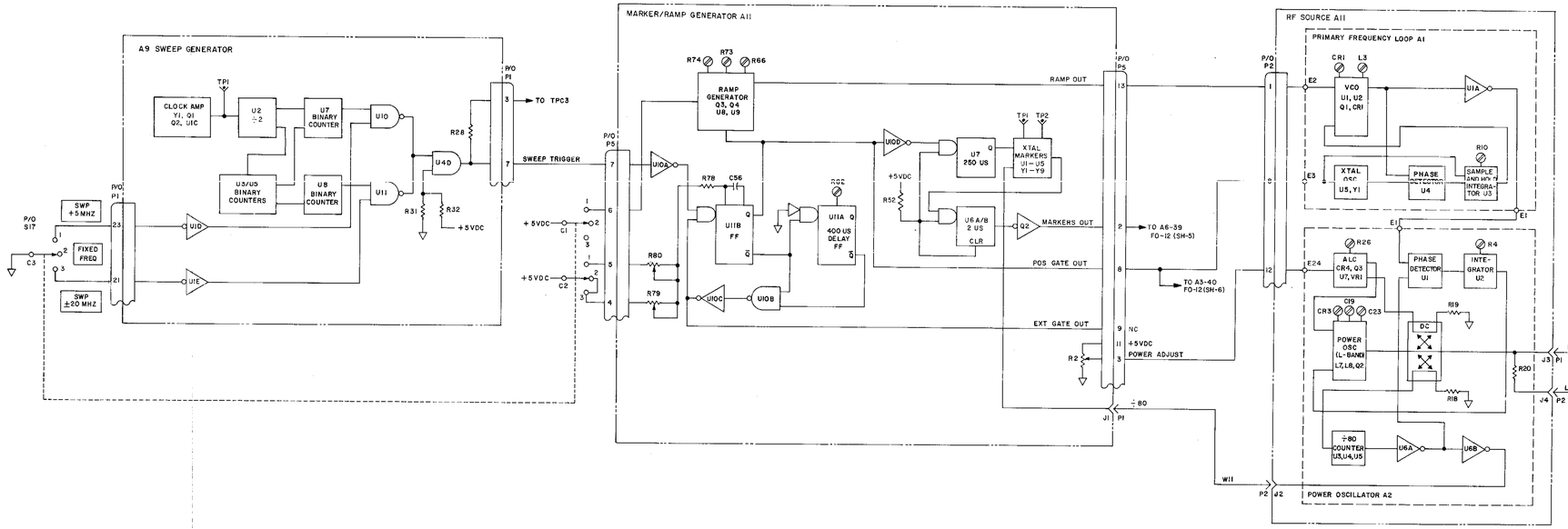
FO-5(2) Video generator logic diagram (sheet 2 of 3).



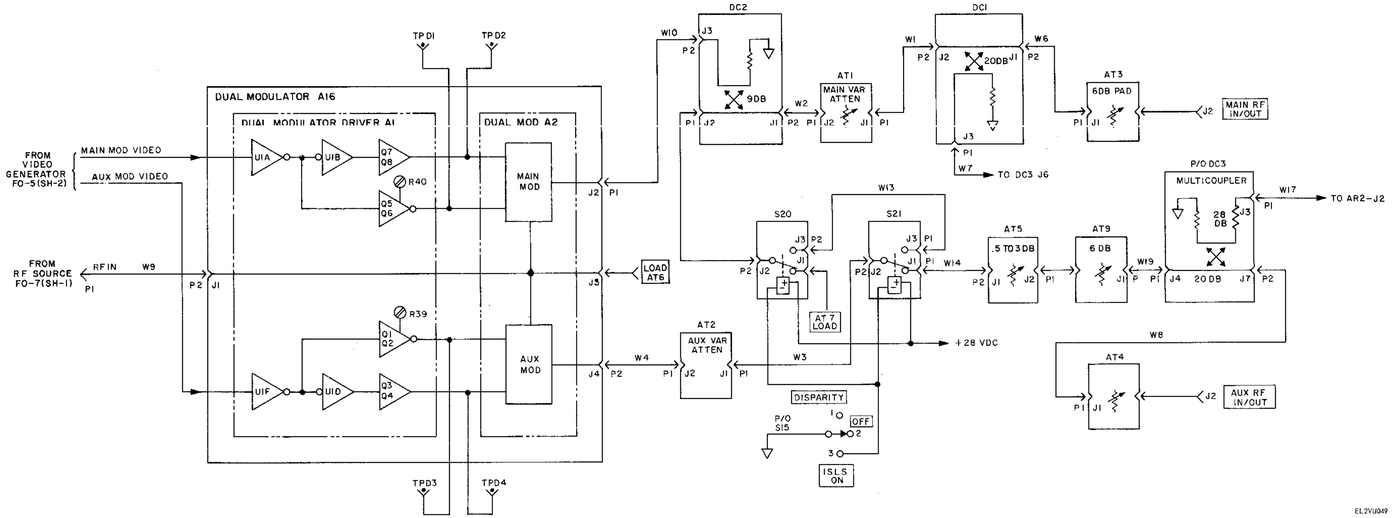
FO-20 Video generator logic diagram (sheet 2 of 3).



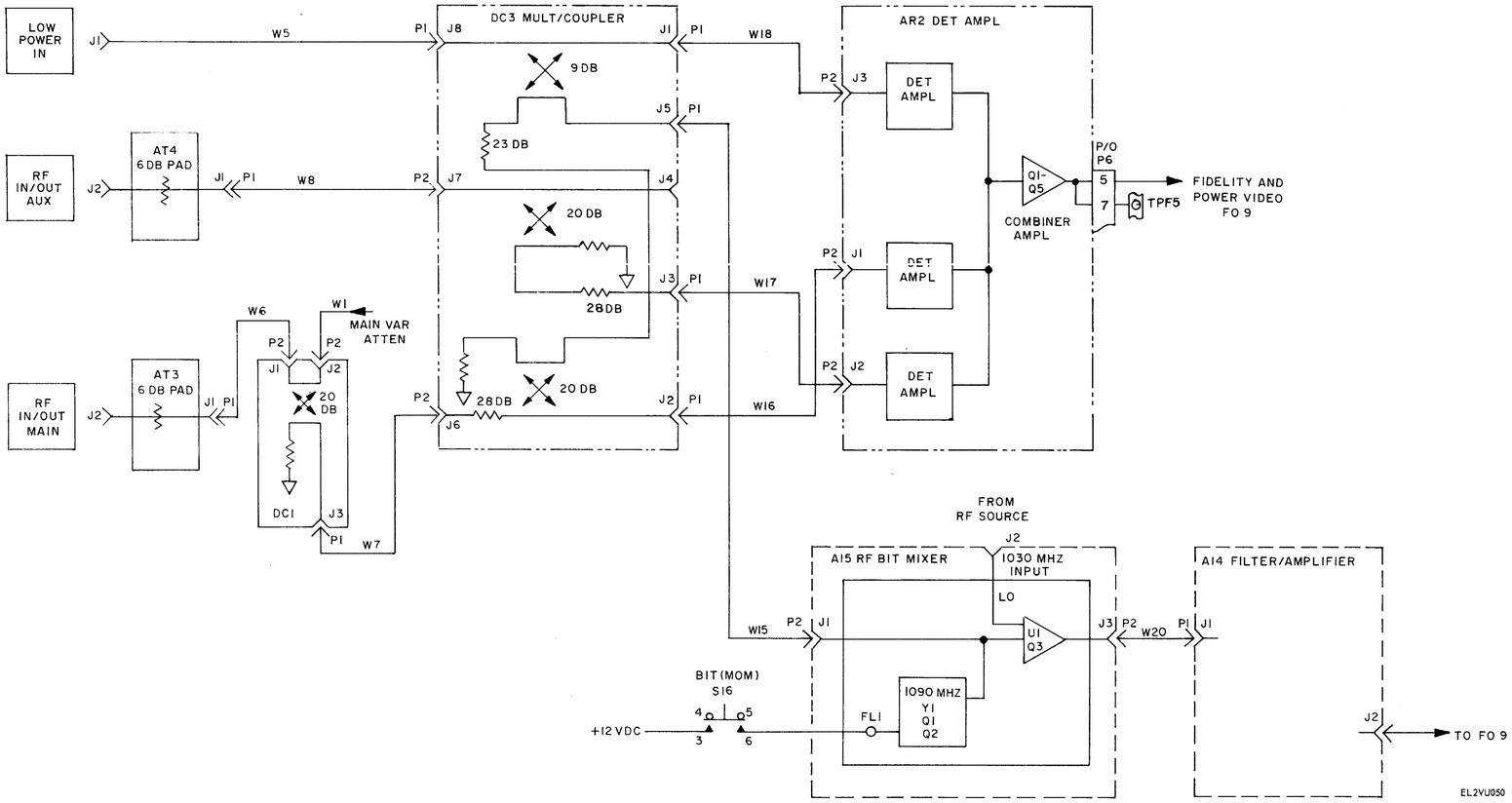
FO-6 *Video generator timing diagram.*



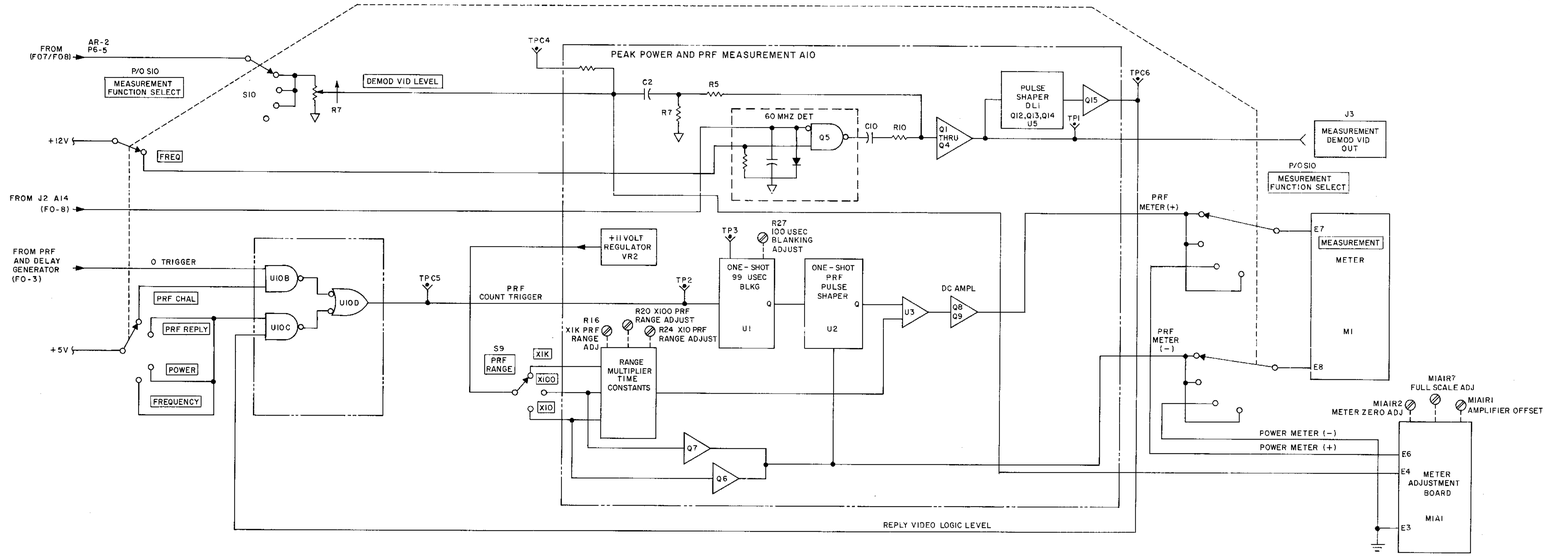
FO-7 RF signal generator data flow diagram (sheet 1 of 2).



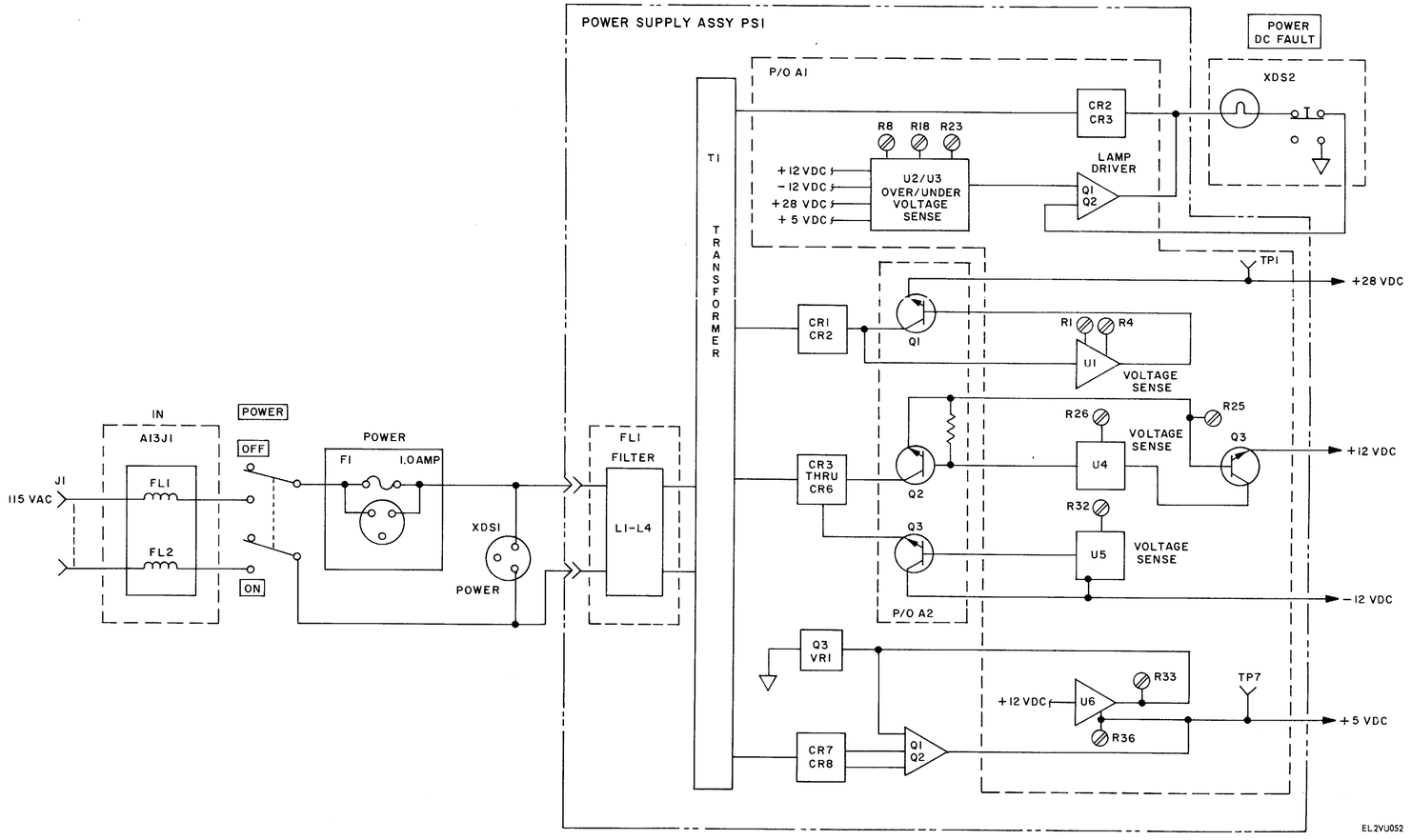
FO-7 Rf signal generator data flow diagram (sheet 2 of 2).



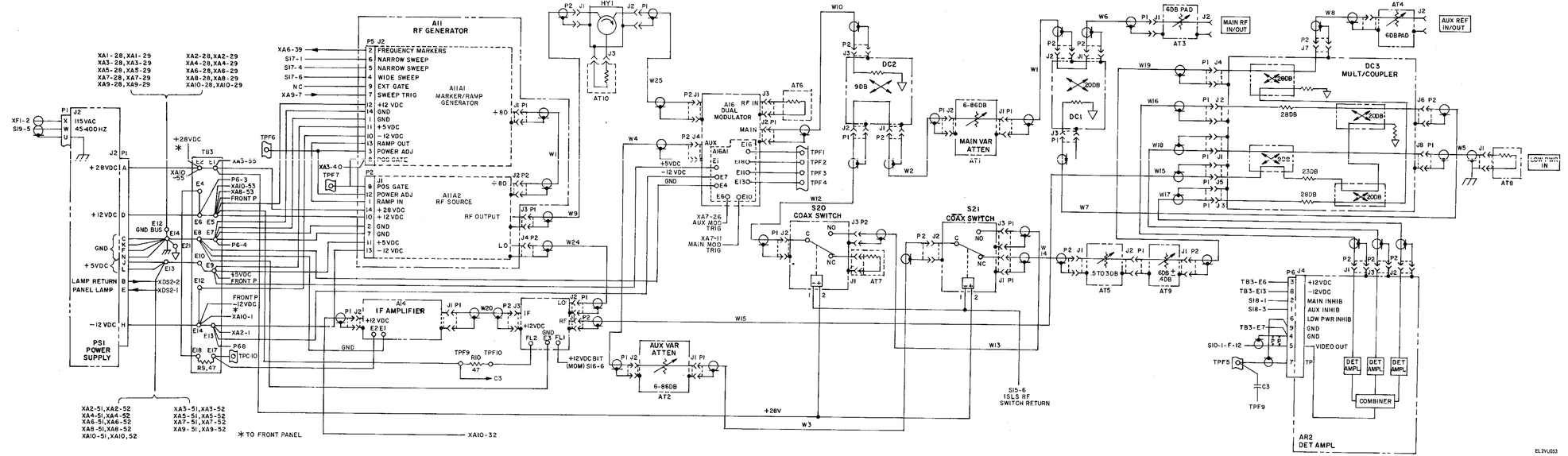
FO–8 Receiver block diagram.



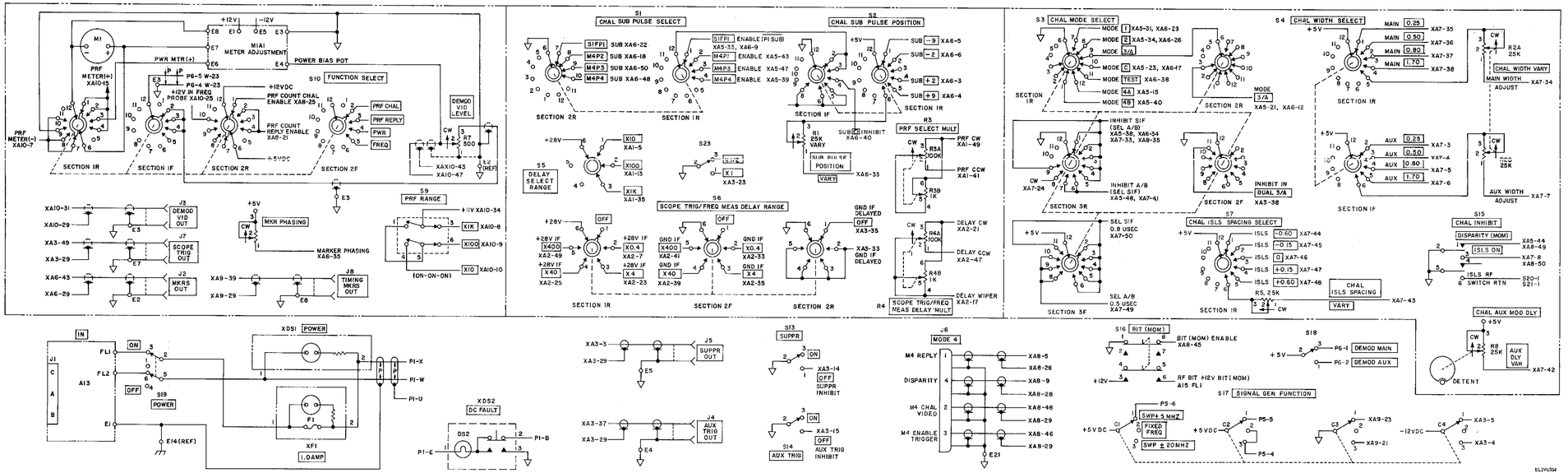
FO-9 Measurement section block diagram.



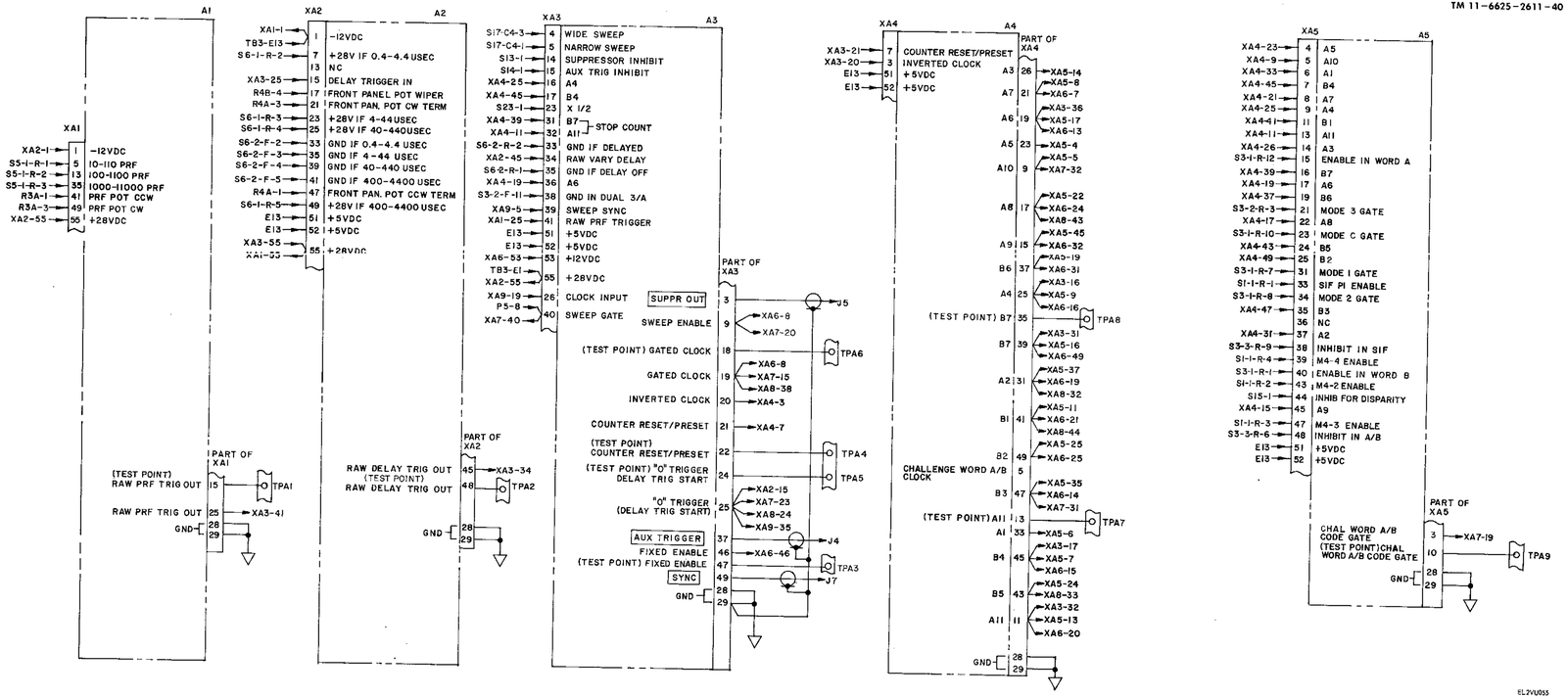
FO-10 Power supply block diagram



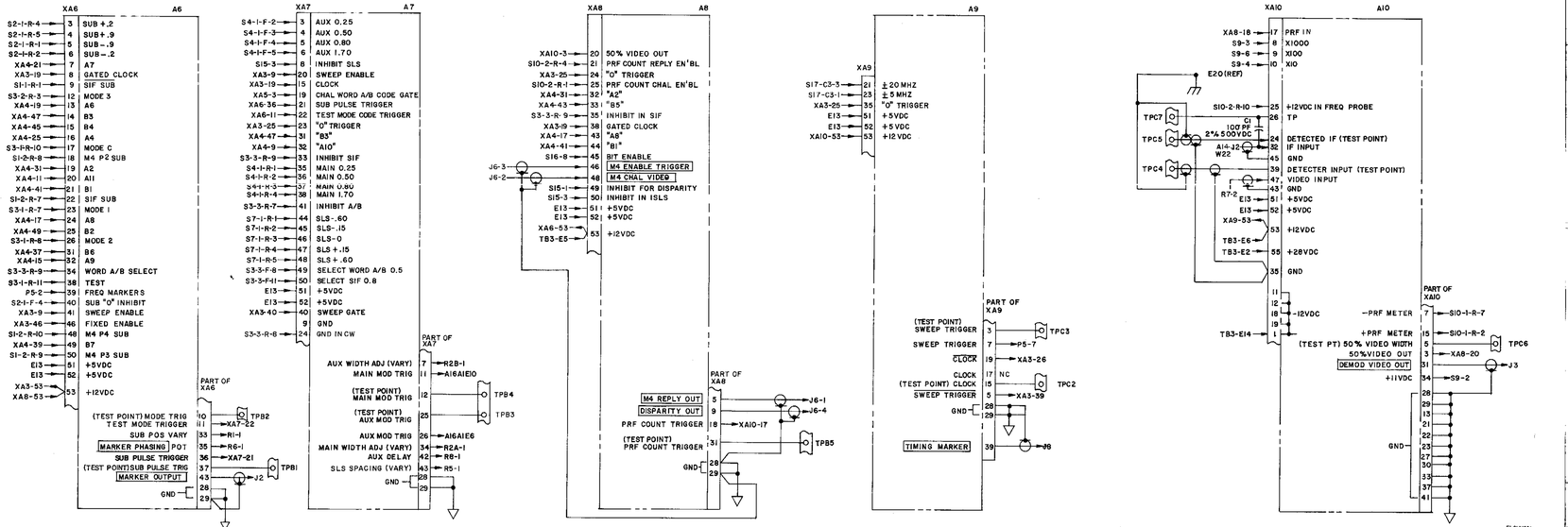
FO-11(1) *Test set schematic diagram (sheet 1 of 4)*



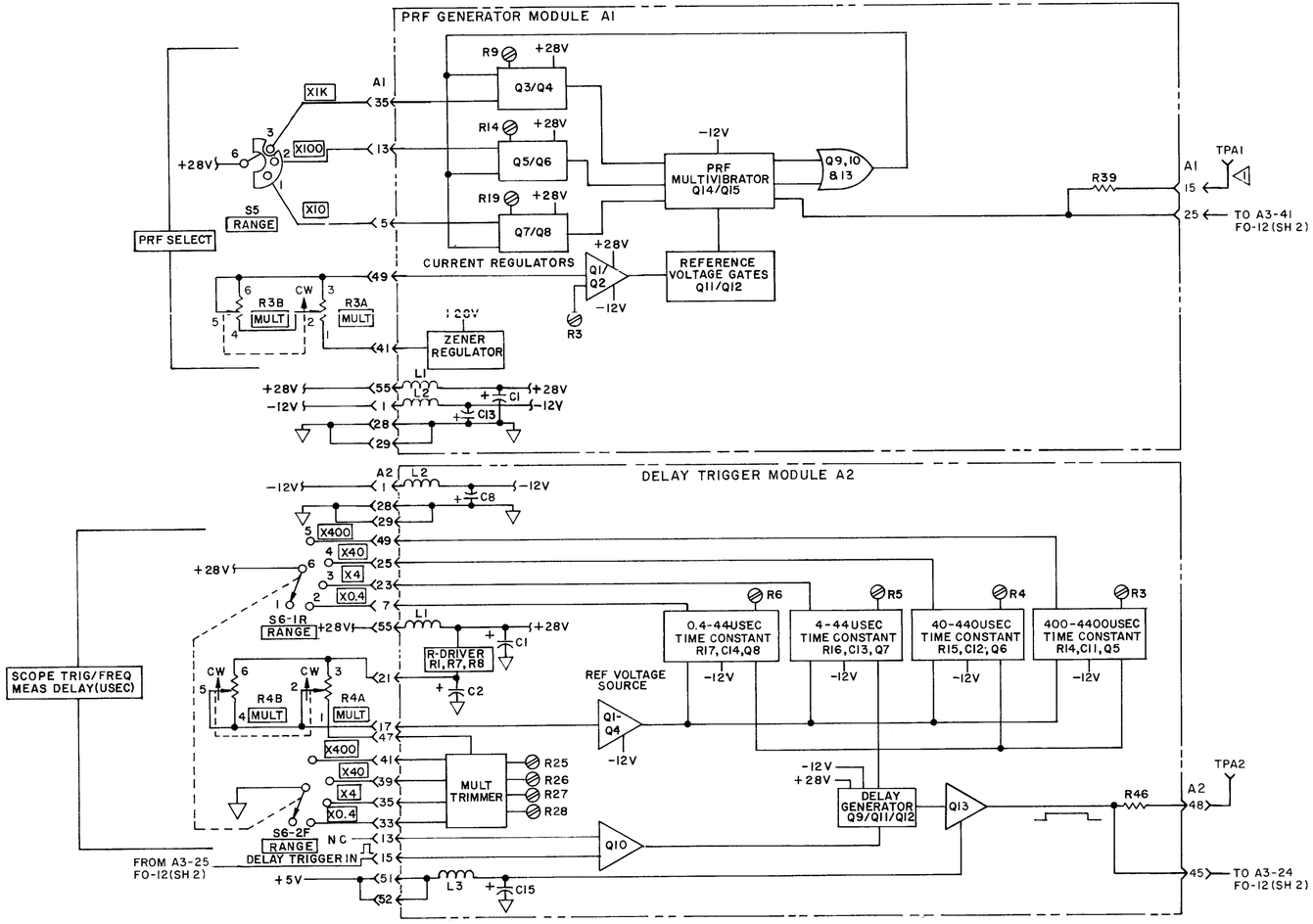
FO-16 Test set schematic diagram (sheet 1 of 4).



FO-11(2) Test set schematic diagram (sheet 3 of 4).



FO-11 Test set schematic diagram (sheet 1 of 4).

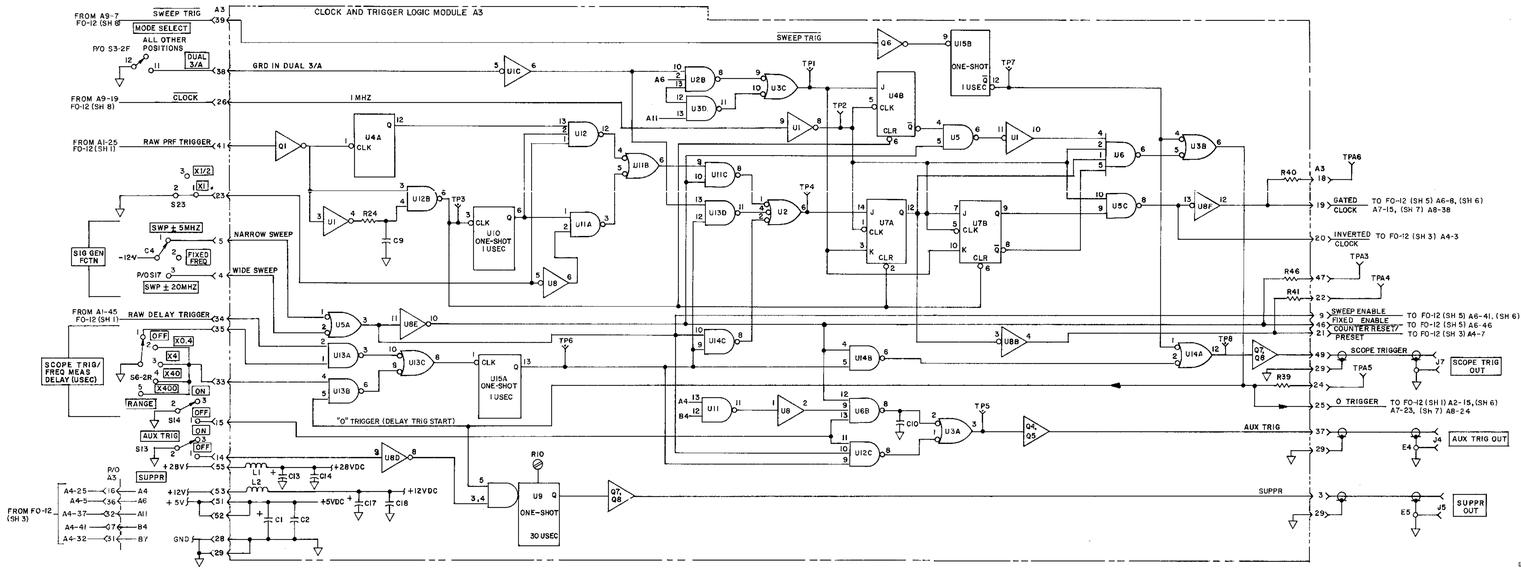


NOTES:

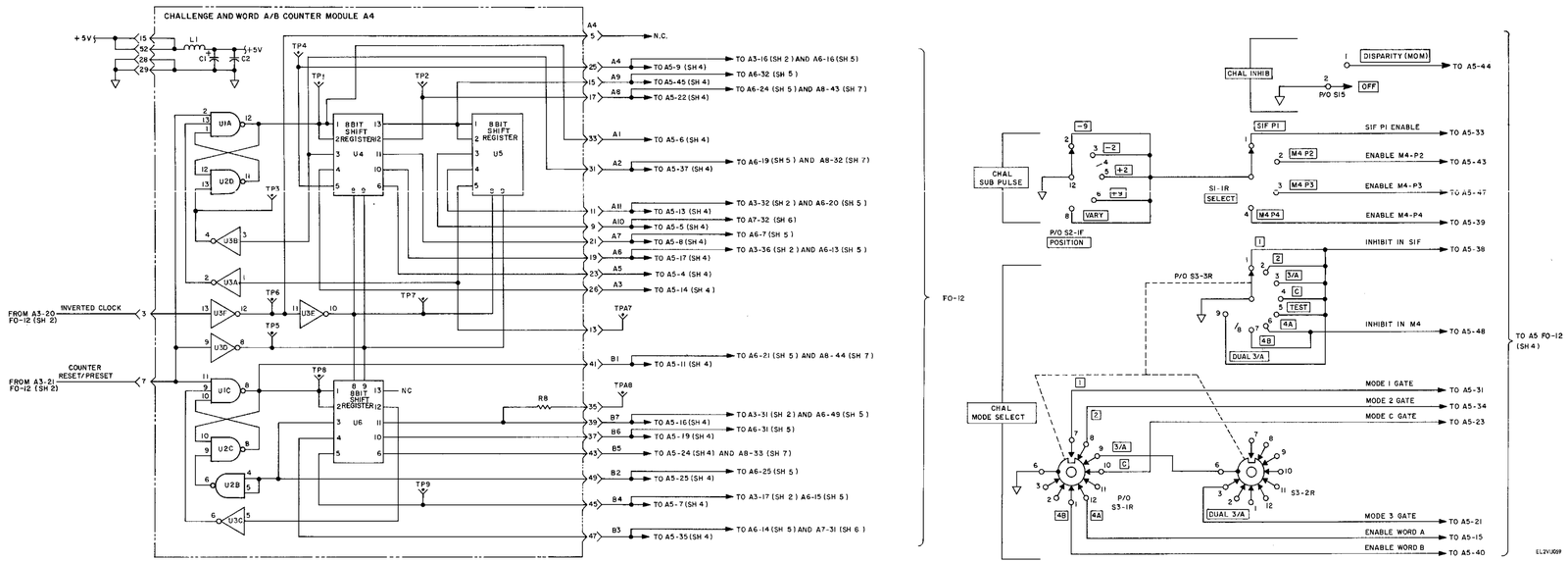
1. ◁ THESE TEST POINTS ARE TO BE USED DURING SELF-TEST OPERATIONS IN ADDITION TO ALL INPUT AND OUTPUT CONNECTIONS ON FRONT PANEL OF UNIT.

EL2VU057

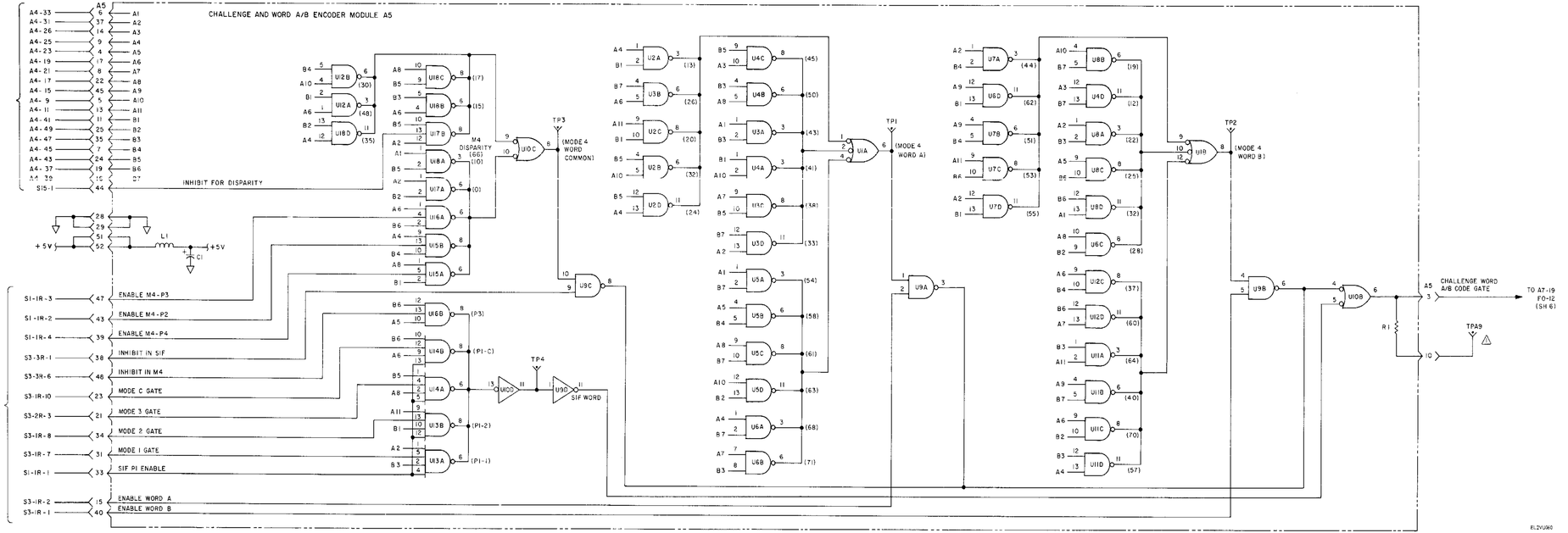
FO–12 (1) Troubleshooting logic diagram (sheet 1 of 8)

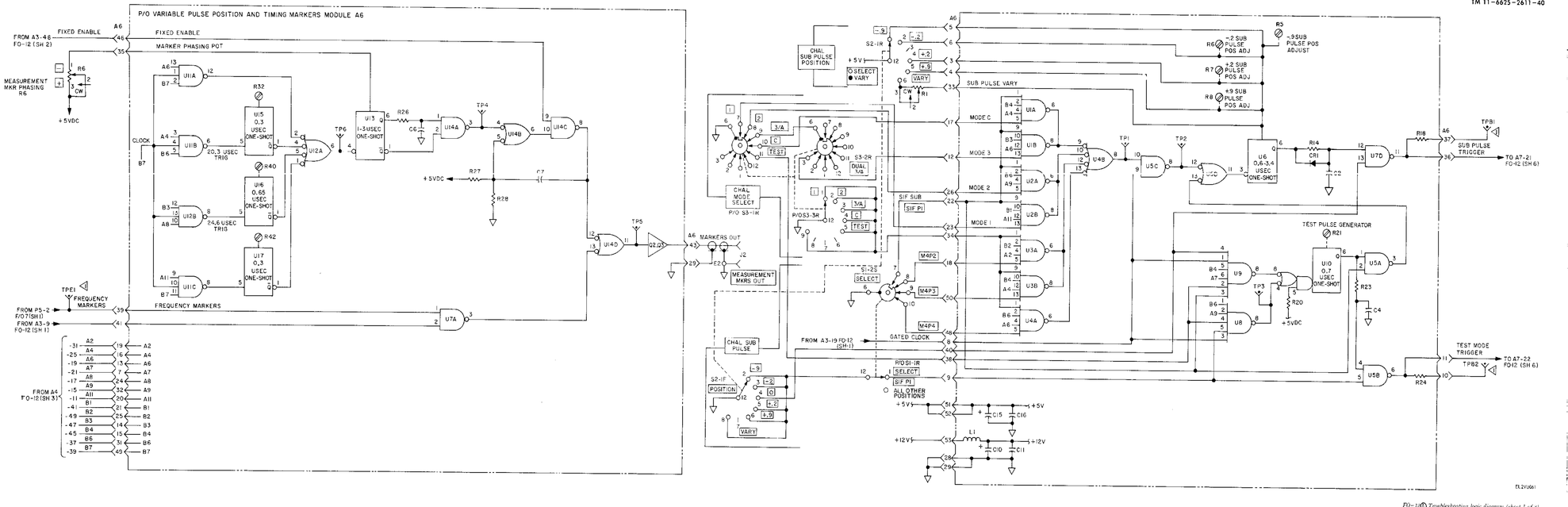


FO-15 Troubleshooting logic diagram (sheet 2 of 8).

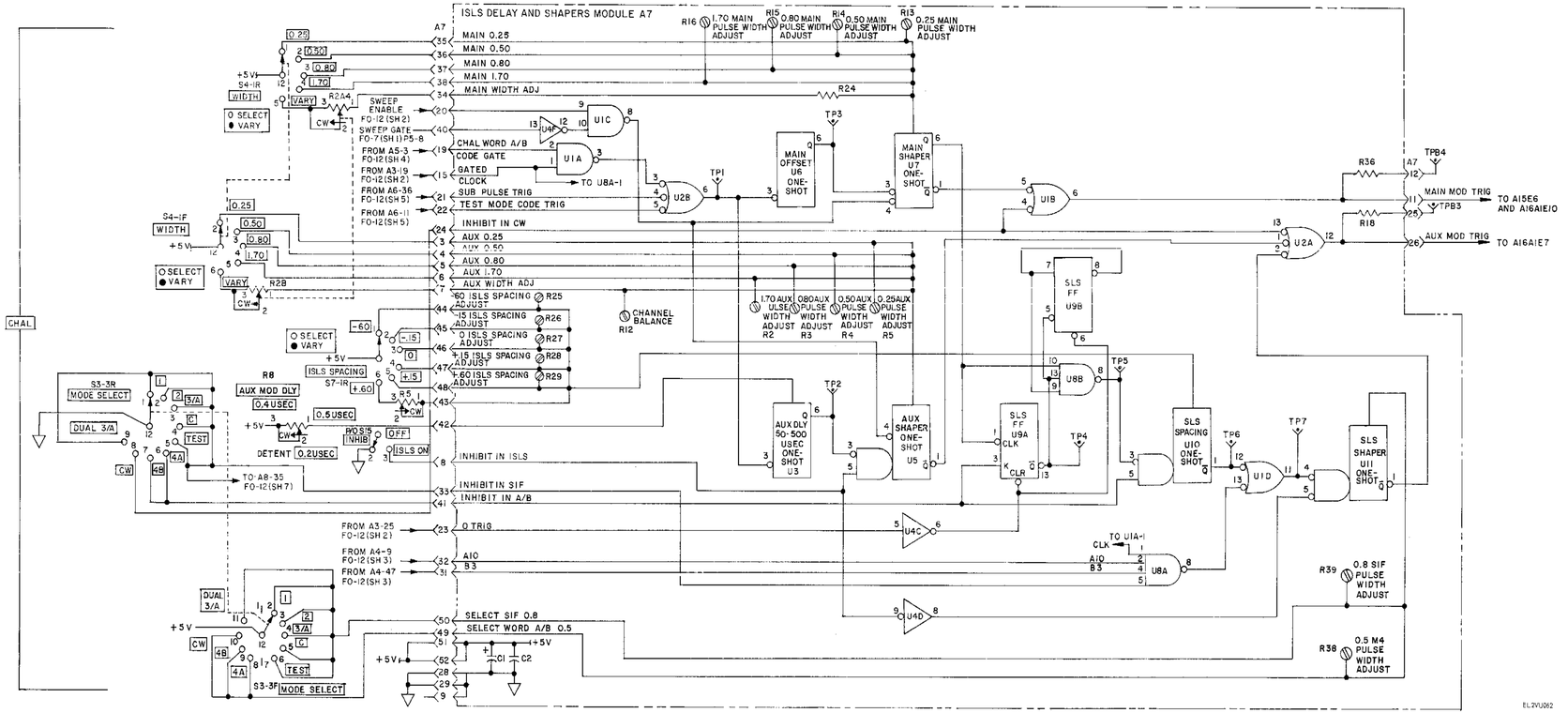


FO-12 Troubleshooting logic diagram (sheet 3 of 8).

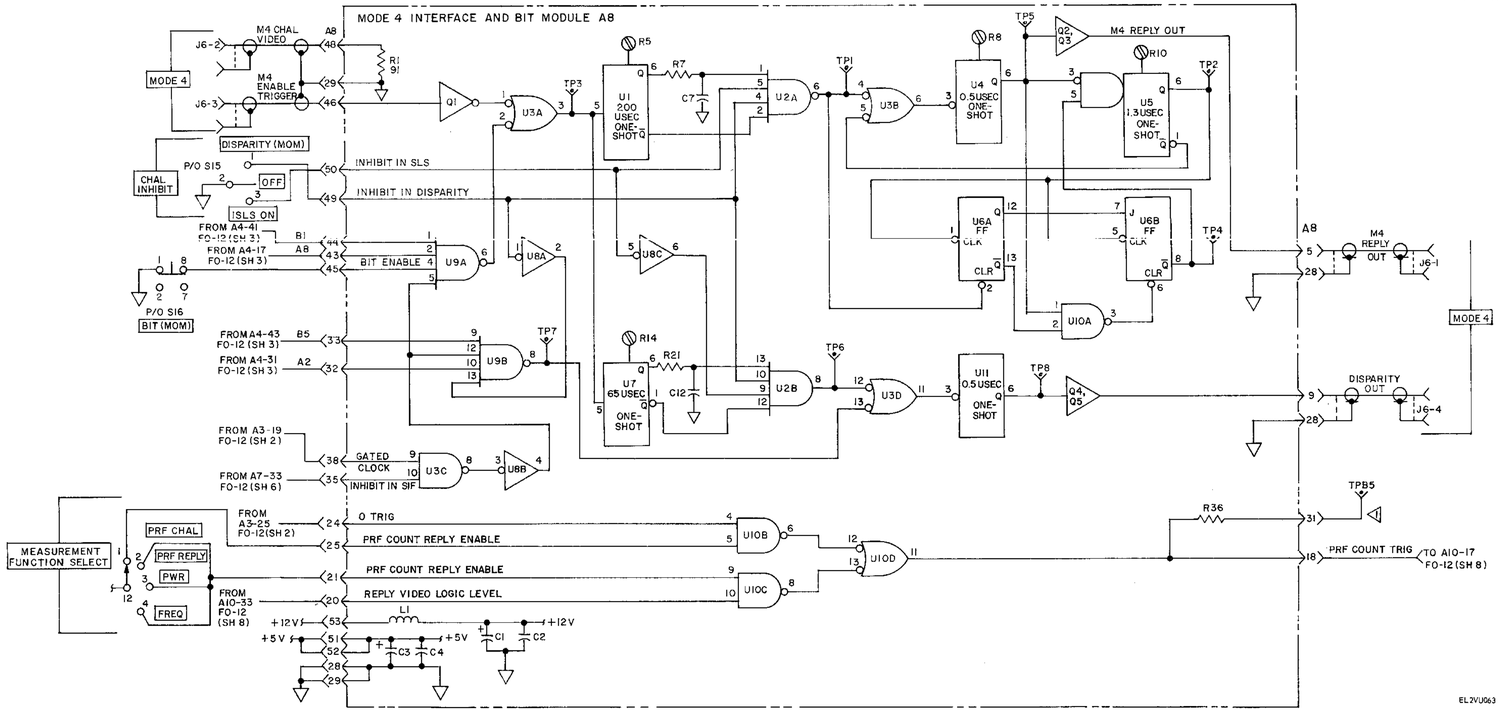

CHALLENGE AND WORD A/B ENCODER MODULE A5
FROM FO-12 (SH 3)
A4-33
A4-31
A4-26
A4-25
A4-23
A4-19
A4-21
A4-17
A4-15
A4-9
A4-11
A4-41
A4-49
A4-47
A4-45
A4-43
A4-37
A4-39
S15-1
A5
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
B1
B2
B3
B4
B5
B6
B7
INHIBIT FOR DISPARITY
+5V
L1
C1
+5V
FROM FO-12 (SH 3)
S1-1R-3
S1-1R-2
S1-1R-4
S3-3R-1
S3-3R-6
S3-1R-10
S3-2R-3
S3-1R-8
S3-1R-7
S1-1R-1
S3-1R-2
S3-1R-1
ENABLE M4-P3
ENABLE M4-P2
ENABLE M4-P4
INHIBIT IN SIF
INHIBIT IN M4
MODE C GATE
MODE 3 GATE
MODE 2 GATE
MODE 1 GATE
SIF PI ENABLE
ENABLE WORD A
ENABLE WORD B
M4 DISPARITY (GG)
(MODE 4 WORD COMMON)
(MODE 4 WORD A)
(MODE 4 WORD B)
CHALLENGE WORD A/B CODE GATE
TO A7-19 FO-12 (SH 6)
SIF WORD
TP1
TP2
TP3
TP4
TP9
R1
ELDVU60



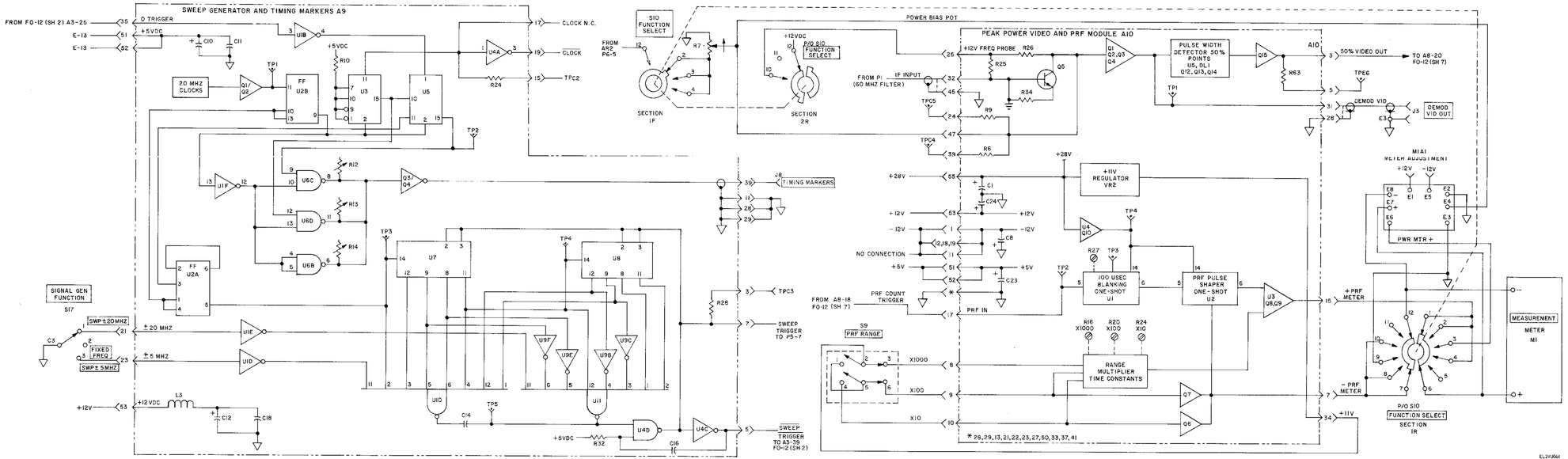
FO-12 Troubleshooting logic diagram (sheet 3 of 4).



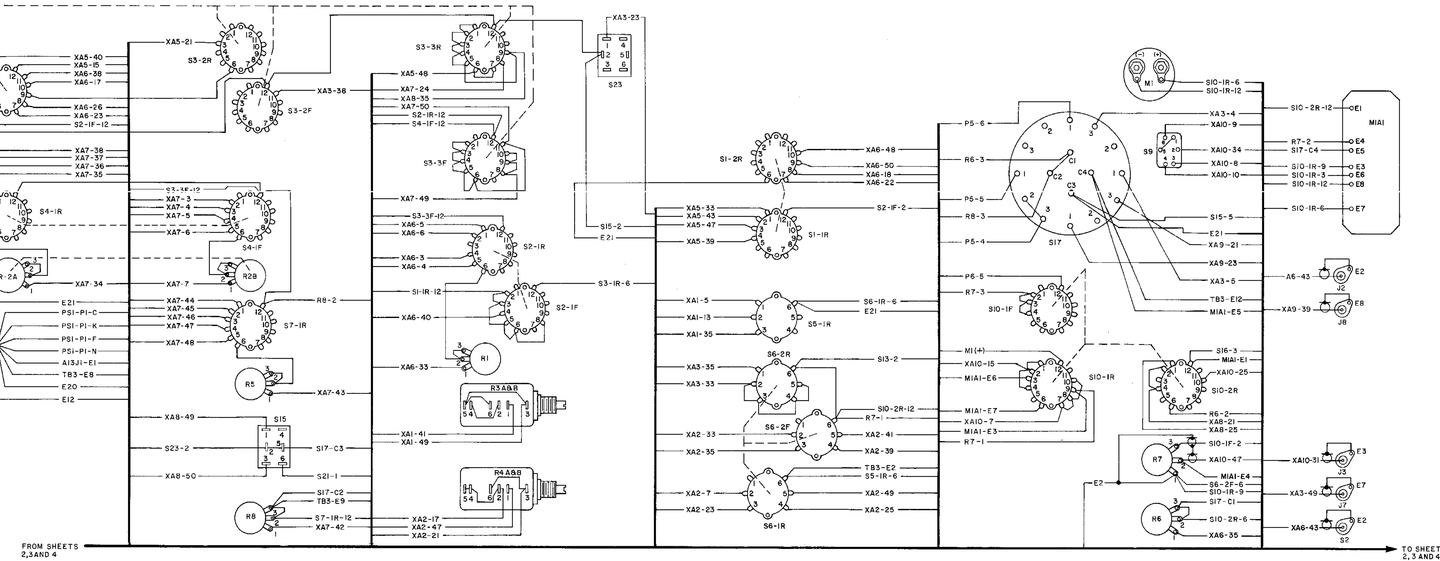
FO-12(8) Troubleshooting logic diagram (sheet 6 of 8).



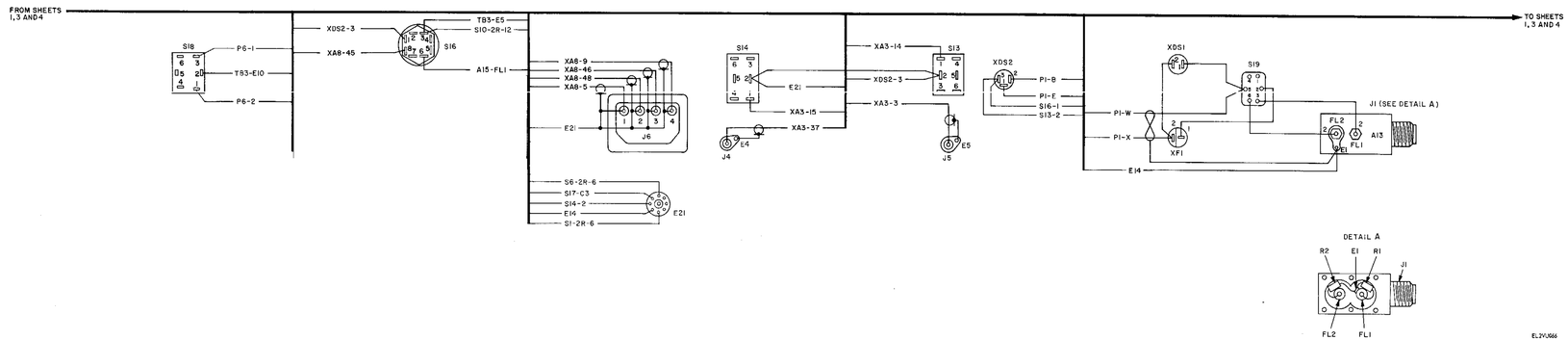
F0-18 Troubleshooting logic diagram (sheet 7 of 8).



FO-12 Troubleshooting logic diagram (sheet 8 of 8).

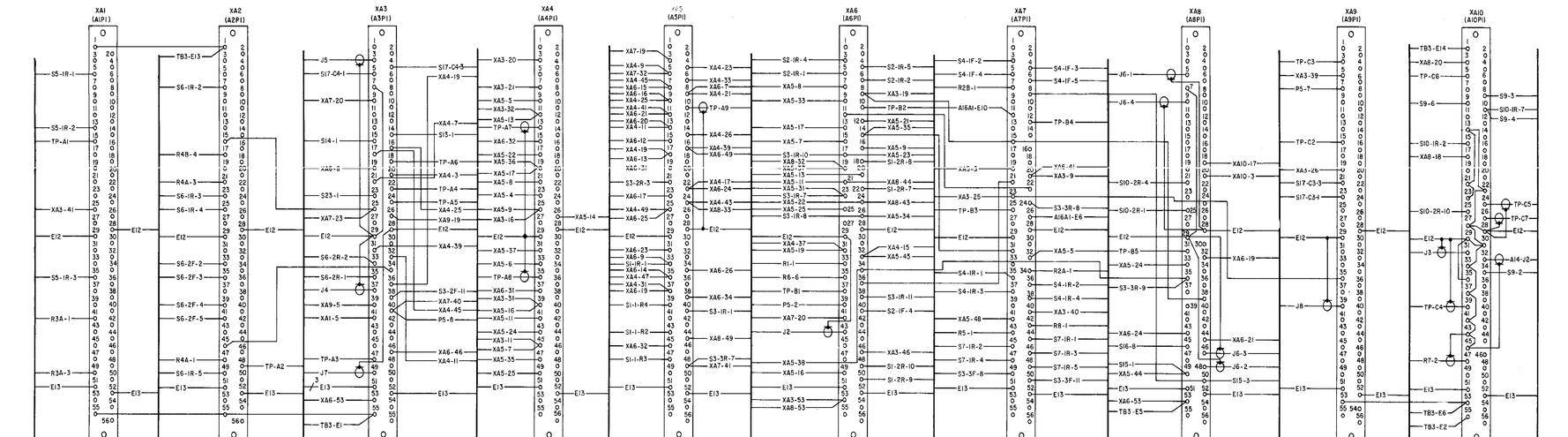


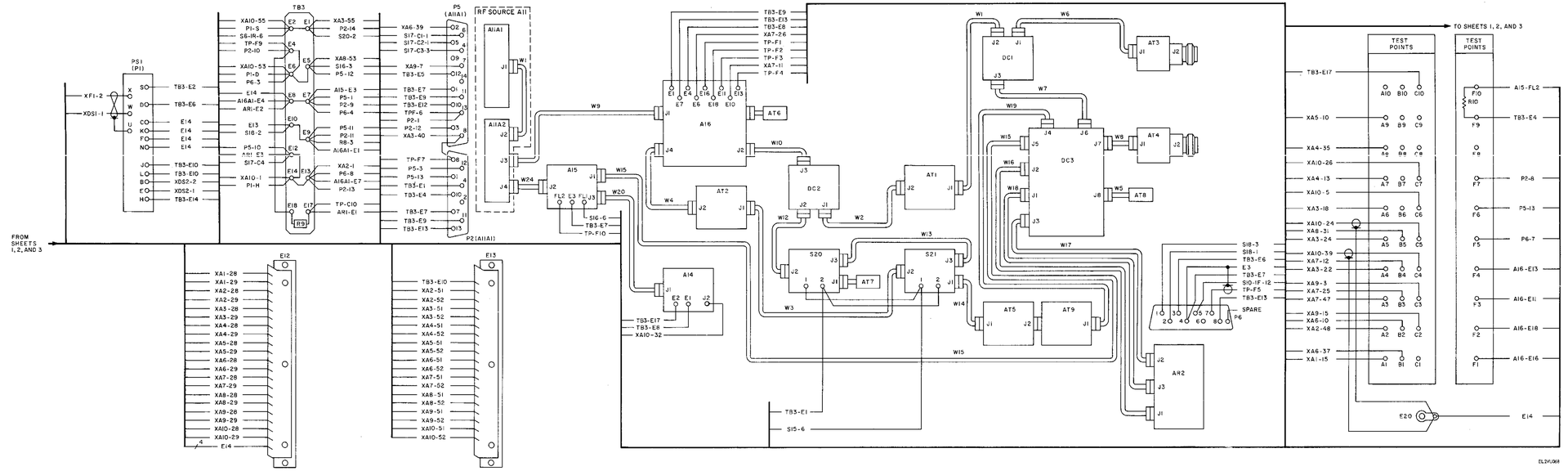
FO-18 Test set wiring diagram (sheet 1 of 4).

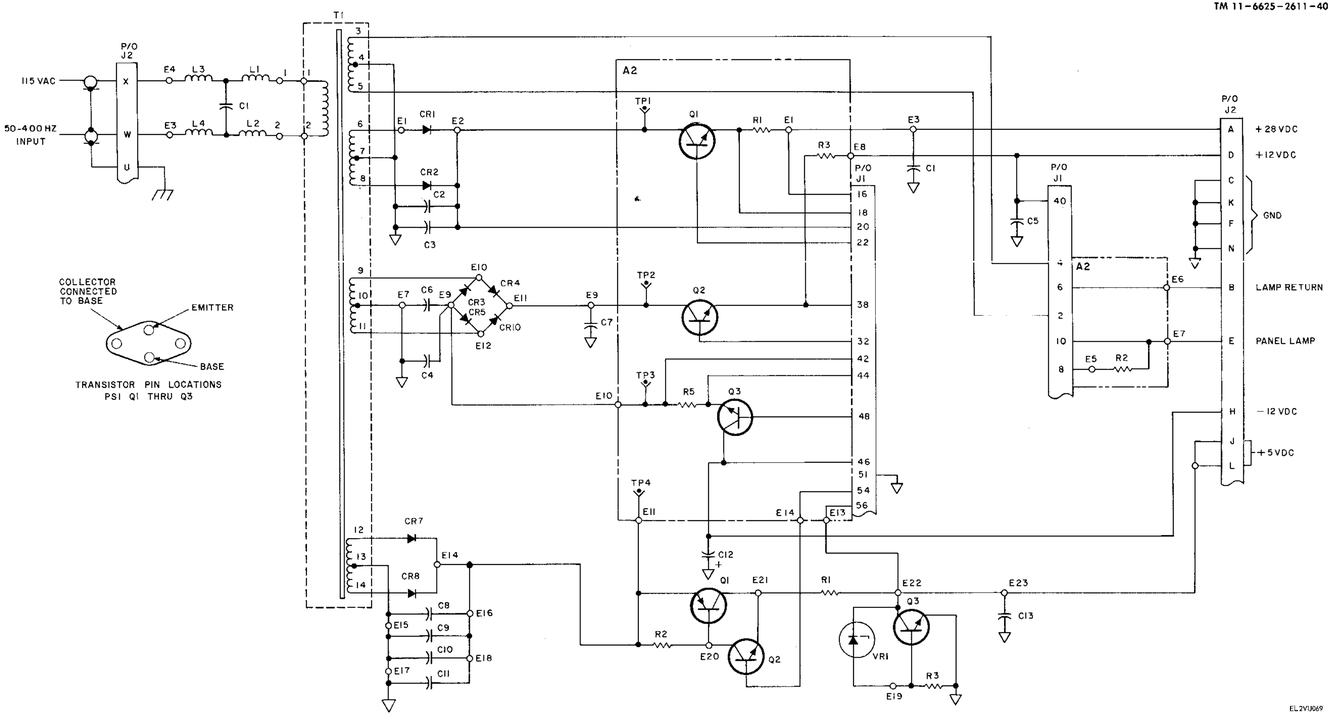


FOLD OUT

FO-18 Test set wiring diagram (sheet 2 of 4)


XA1 (A1P1)
XA2 (A2P1)
XA3 (A3P1)
XA4 (A4P1)
XA5 (A5P1)
XA6 (A6P1)
XA7 (A7P1)
XA8 (A8P1)
XA9 (A9P1)
XA10 (A10P1)
FROM SHEETS 1, 2 AND 4
TO SHEETS 1, 2 AND 4
NOTES:
1. E12, AND E13 ARE BUS BAR.
EL2VJ067


FROM SHEETS 1, 2, AND 3
PS1 (P1)
XF1-2
XDS1-1
TB3
P5 (A11A1)
RF SOURCE A11
A11A1
A11A2
A15
A16
A14
DC1
DC2
DC3
S20
S21
AR2
AT1
AT2
AT3
AT4
AT5
AT6
AT7
AT8
AT9
R89
E12
E13
P2(A11A1)
TB3-E9
TB3-E13
TB3-E8
XA7-26
TP-F1
TP-F2
TP-F3
XA7-11
TP-F4
TB3-E17
TB3-E8
XA10-32
TB3-E1
SI5-6
SIG-G
TB3-E7
TP-F10
SI8-3
SI8-1
TB3-E6
E3
TB3-E7
SI0-1F-12
TP-F5
TB3-E13
SPARE
P6
TO SHEETS 1, 2, AND 3
TEST POINTS
TEST POINTS
E20
E14
EL2VL068



FO-14 Power supply schematic diagram.

By Order of the Secretary of the Army:

BERNARD W. ROGERS
General, United States Army
Chief of Staff

Official:

J. C. PENNINGTON
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Ft Richardson (CERCOM) (2)
Army Dep (1) except
LBAD (14)
SAAD (30)
TOAD (14)
SHAD (3)
USA Dep (1)
Sig Sec USA Dep (1)
Units org under fol TOE:
(1 cy each unit, UNOINDC)
29-207 (2)
29-610 (2)
29-134
44-536
55-457

NG: None
USAR: None
For explanation of abbreviations used, see AR 310-50.

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