TECHNICAL MANUAL

DIRECT SUPPORT

MAINTENANCE MANUAL

INVERTER, POWER, STATIC

PP-7274C/A

(NSN 6125-00-148-8342)

(GULTON INDUSTRIES

MODEL EMIR283A)

HEADQUARTERS, DEPARTMENT OF THE ARMY
19 MAY 1982

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3 IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

4 SEND FOR HELP AS SOON AS POSSIBLE

5 AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNINGS

Personnel performing instructions involving operating procedures and practices which are included or implied in this technical manual shall observe the following precaution. Disregard of these warnings and precautionary information may result in injury, death or an aborted mission.

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. rolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

Compressed air shall not be used for cleaning purposes except where reduced to less than 29 pounds per square inch (psi) and then only with effective chip guarding and personnel protective equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skinof the operator or other personnel.

HAZARDOUS VOLTAGES AND HIGH CURRENT

To avoid electrical shock be extremely careful when making required measurements and adjustments. Ensure all power is off when disassembling or assembling inverter.

Technical Manual

No. 11-6125-259-30

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON DC, *19 May 1982*

DIRECT SUPPORT MAINTENANCE MANUAL
INVERTER, POWER, STATIC PP-7274C/A
(NSN 6125-00-148-8342)
(GULTON INDUSTRIES MODEL EMIR283A)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703.

In either case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. scope

This manual contains information and maintenance instructions of the Static Power Inverter (inverter) (Gulton Industries, Engineeered Magnetics Division Model EMIR283A (Part No. 524595)). The inverter is designed in accordance with military Specifications MS17406-3C. It is qualified for use in military aircraft.

1-2. Index of Technical Publications

Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

1-3 Maintenance Forms, Records, and Reports

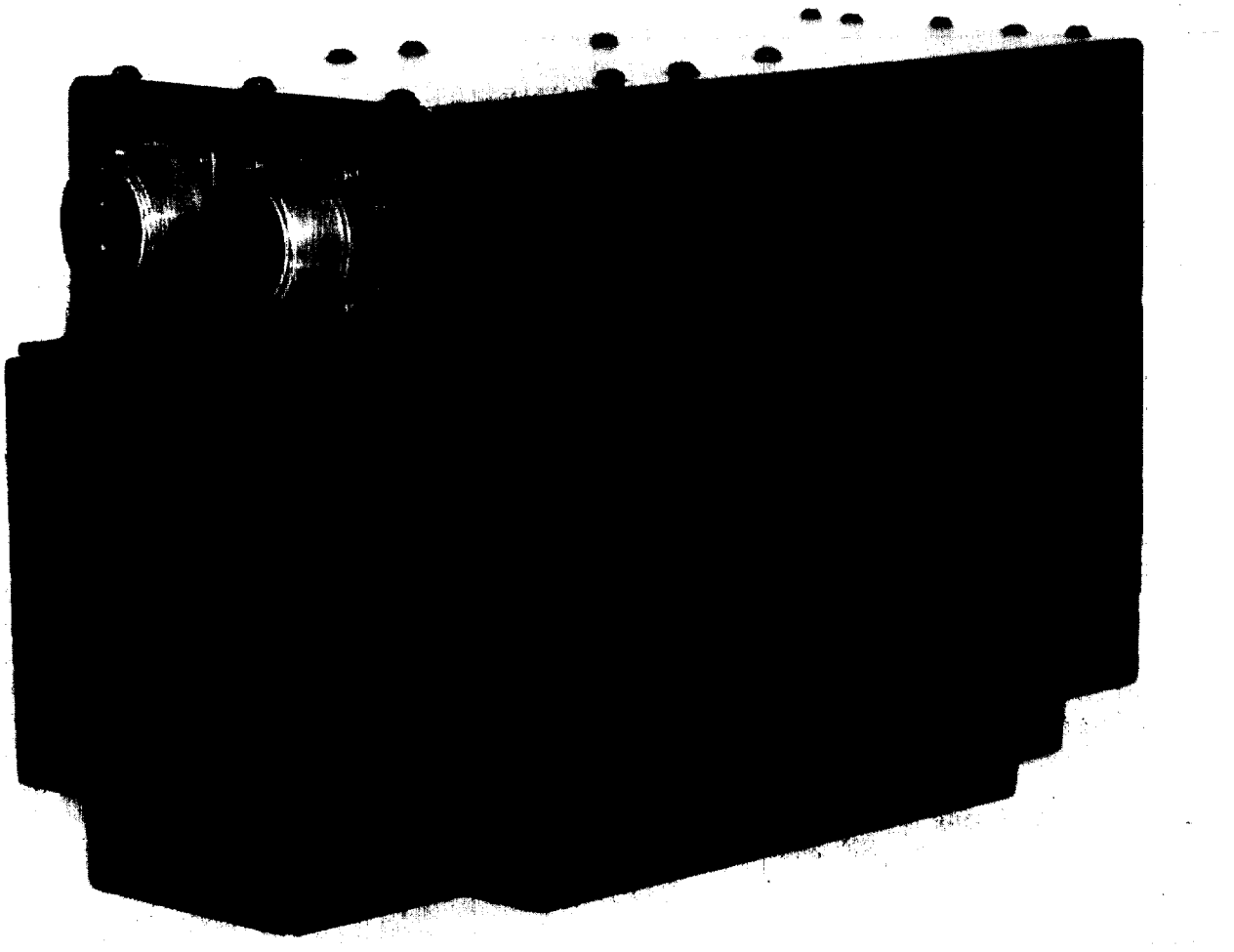
a. Reports of maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be TM 38-750, The Army Maintenance Management system.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73 AFR 400-54/MCO 4430.3E

c. Discrepancy in Shipment Report (DISREP) (SF 361) Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) AS PRESCRIBEDF IN AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19c/dlar 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

If your Static Power Inverter PP-7274C/A needs improvement, let us know. Send us an EIR. You the user, are the only one who can tell us what you don't like about your equipment. Let us knmow why you don't like the design. Tell us why a procedure is hard to perform. PUt it on an SF 368 (Quality Deficincy Report). Mail it to Ccommander, US Army Communications-Electronics Command, ATTN: DR-SEL-ME-MQ, Fort Monmouth, NJ 07703. We'll send you a reply.



EL7PI001

Figure 1-1. Inverter, Power, Static PP-7274C/A.

1-5 Warranty

This equipment is under a two year warranty with the contractor. Check the data plate for expiration date of warranty (two years from date on warranty plate). If the inverter is still under warranty, return the inverter directly to the contractor using the address provided on the data plate.

1-6. Destruction of Army E1ectronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Section II. DESCRIPTION AND DATA

1-7. Description

The inverter (fig.1-l) operates on a 28 volt nominal dc input and suppliea a 115 vac rms output, 3 phase, 400 Hz. The output can be connected to a load in either way or delta configurations as shown in figure 1-2. This highly reliable inverter is installed for air borne use and accommodates loads of up to 250 va for each phase (750 va total). It is a rugged, light-

weight, modularized inverter and contains solid state circuits throughout. The inverter is self-cooled by natural convection, conduction, radiation and an internal fan.

1-8. Tabulated Data

Input Voltage:	18 to 29 vdc (28 vdc at 17.4 amps, nominal)
Output voltage:	115 vac rms, nominal, at 2.17 amps 112.5 to 117.5 vac rms (at 26 to 29 vdc input), 3Ø 100.0 to 117.5 vac rms (at 18 to 26 vdc input,) 3Ø
Output Power:	250 va at 0.75 amps per phase
Output Frequency:	393 to 407 Hz (at 18 to 29 vdc input)
Phase Rotation:	ABC
Output Full Load:	250 va phase, 750 va total, 0.75 PF minimum lagging
Minimum Efficiency:	65% at full load (unit PF) and 28 vdc input, room ambient
Output Distortion	5% maximum phase (at 18 to 29 vdc input)
Amplitude Modulation:	3.25 volts peak-to-peak maximum
Overload and Short Circuit Protected:	15 minutes, recovers within 2 seconds after removal of overload or short circuit
Operating Altitude:	To 50,000 feet, rated power To 65,000, half rated power minimum
Operating Temperatures:	-56° to +85°C
Dimensions (max):	11-1/2 inches long 5-1/2 inches wide 8 inches high
Mounting:	Four 0.397-inch diameter holes, 4 X 5-inch centers
Weight:	23 lbs maximum
Connectors:	J1, type MS3102R22-6P J2, type MS3102R22-5S
Test Points:	Measures output voltage, located adjacent to J2
Input Connector, J1, pins:	A (-) C (+) B Not Used
Output connector, J2, pins:	AØA, BØB, CØC } 3Ø Output DØB, EØC, PØA } Output Return

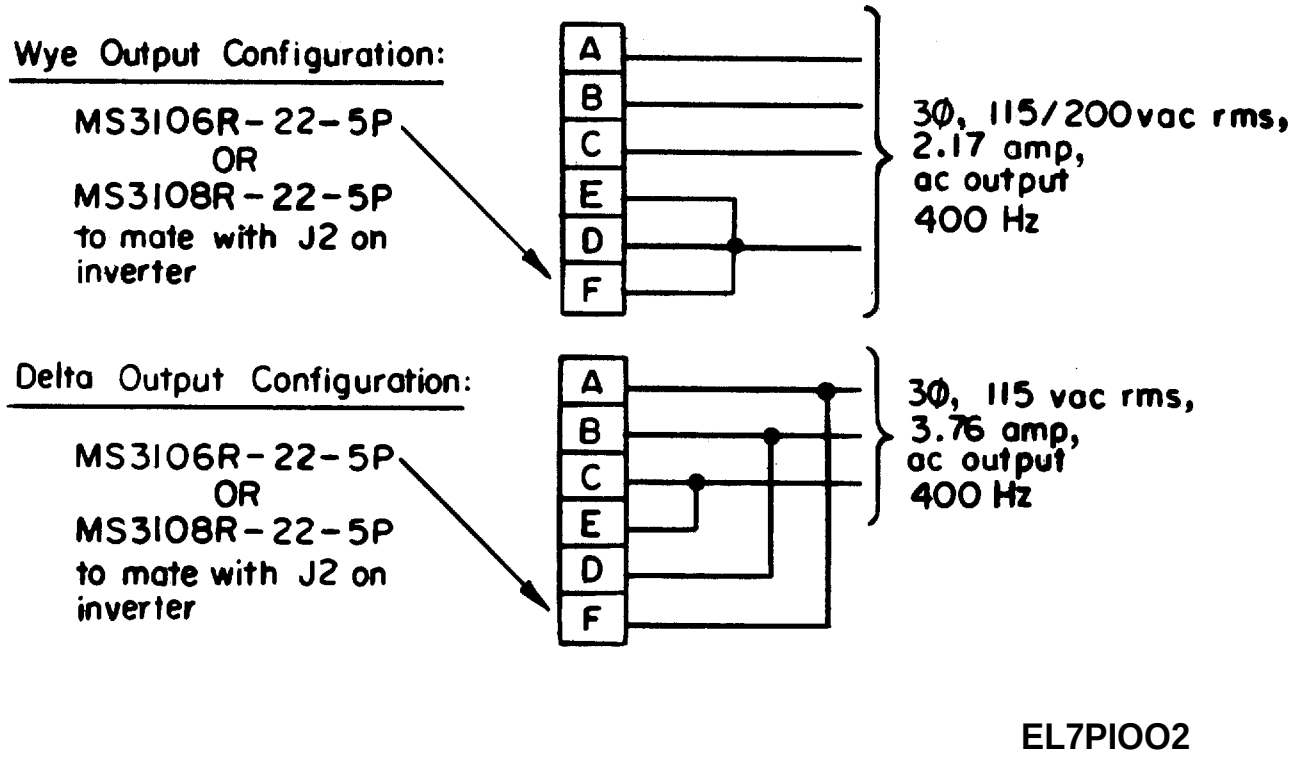


Figure 1-2. Output Connection Configurations.

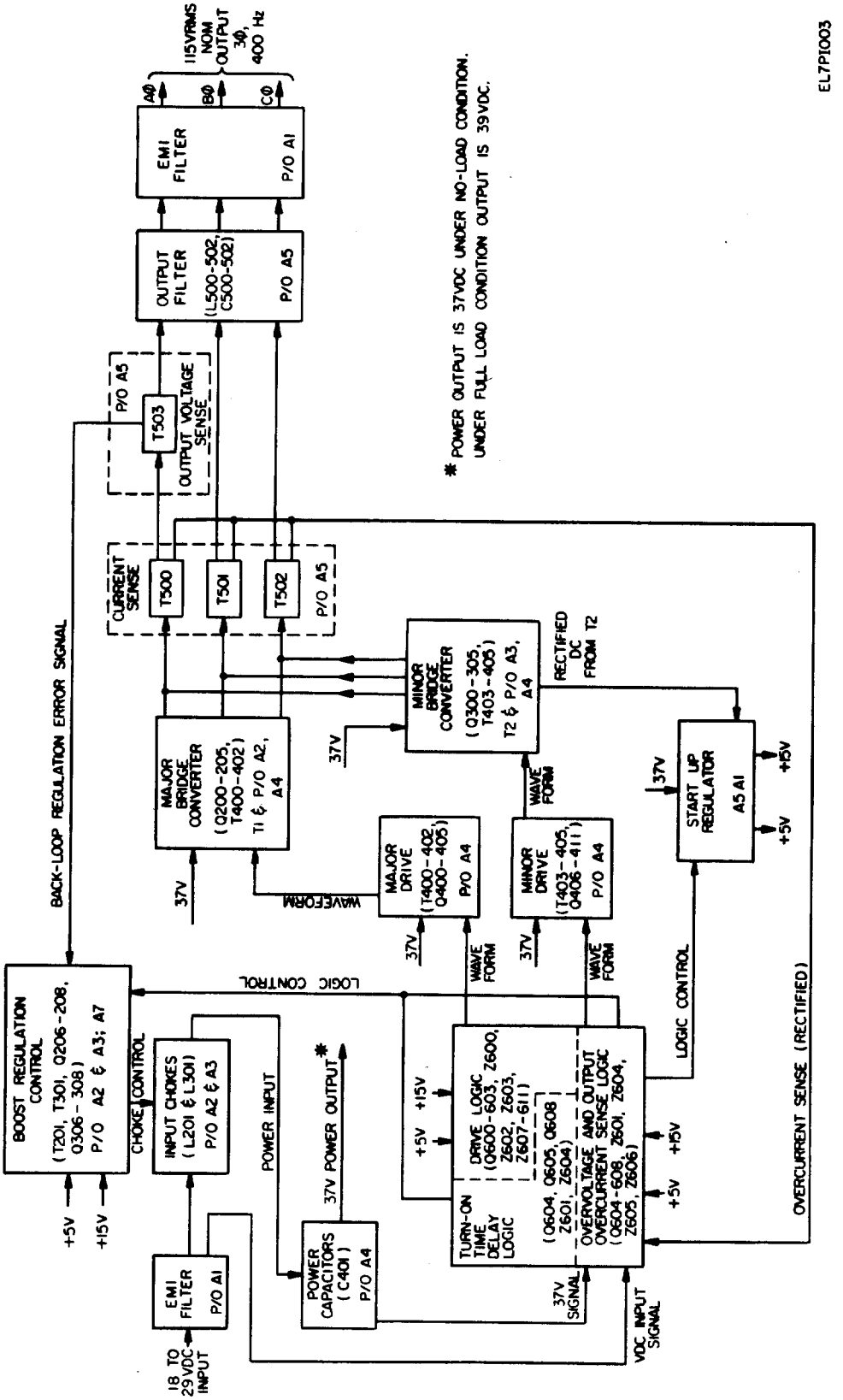


Figure 2-1. Block Diagram.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

2-1. Static Inverter Block Diagram Functional Description

The inverter, consists of the following subassemblies and sections (see block diagram, fig. 2-1): Input and Output EMI Filters. Start Up Regulator, Boost Regulation Control, Input Chokes, Power Capacitors, Logic, Overvoltage Sense, Overcurrent Sense, Major and Minor Drive, Major and Minor Bridge Converters, Output Voltage Sense, and Output Filter.

a. Input EMI (Electromagnetic Interference) Filter. The EMI filter reduces conducted and radiated energy.

b. Start Up Regulator. The start up regulator provides regulated +5 vdc and +15 vdc bias voltages to the logic circuits and the boost regulation control. At turn-on, the start up regulator receives its input power from the power capacitors. After turn-on the start up regulator receives its input from rectified voltages from the minor bridge converter transformer T2.

c. Boost Regulation Control. This overall regulation circuit consists of part of the A2 assembly (high level boost) and A3 assembly (low level boost) and the entire A7 assembly (boost regulator). The A2 and A3 assemblies function in an identical way in this circuit; each one servicing an input choke (L201, L301). The overall circuit regulates the 37 vdc supply. The regulation is accomplished by changing the duty cycle ratio (choke charge time to choke discharge-into-power-capacitors time) of the two input chokes which feed into the power capacitors to form the 7 vdc supply. The duty cycle ratio is proportional to the input voltage and the inverter output load. The A7 boost regulator alternately acts to charge and discharge the two input chokes into the power capacitors in order to create a push-pull effect. The circuit also makes use of a power ratio transfer (low voltage_high current versus high voltage_low current) and, in addition, the circuit receives an error signal from the output voltage sense circuit and this back-loop regulation enables fine control of the 37 vdc and the output ac voltage.

d. Input Chokes. The two input chokes are connected to the inverter input voltage on one end and to the power capacitors on the other end. The boost regulator alternately provides a low impedance to ground (referred to as a short to ground in the text) for the center tap of the two input chokes, which with this high current flow stores energy. During the next cycle of operation the choke energy is discharged into the power capacitors.

e. Power Capacitors. The power capacitors are charged by the energy stored in the input chokes. The 37 vdc output of the power capacitors is used by the major and minor drive circuits, the major and minor bridge converter circuits and initially for power for the start up regulator.

f. Logic. The logic circuit functions as follows: logic to prduce major and minor drive waveforms, turn-on time delay logic, input overvoltage logic and output overcurrent sense logic. The drive logic develops waveforms from a 9.6 KHz oscillator that are fed to the major and minor drive circuits to finally produce major and minor quasi sine waveforms that are fed to output voltage transformers T1 and T2. At inverter turn-on, the +15 V comes on at once and the turn-on time delay logic generates a signal which allows the other circuits to stabilize before the drive waveforms and the +5 vdc and 37 vdc supplies are energized. The input overvoltage logic generates inverter shutdown signals for the major and minor bridges (cuts off the drive waveforms) and turns off the 37 vdc supply. The output overcurrent sense logic maintains a 7.5 amp inverter output current for five seconds after an overload current of 200% or greater (output short circuit) is detected. The inverter output is then cycled off and on until overcurrent condition is removed.

g. Overvoltage Sense. The overvoltage sense circuit detects an excessive (44 vdc) level of inverter input voltage or 37 vdc supply voltage in the form of transient or static potentials. The overvoltage sense circuit will shut down the inverter output and the 37 vdc supply for the duration of the overvoltage.

h. Overcurrent Sense. The overcurrent sense circuit provides inverter protection from overloads greater than 200% and support output short circuit current at 2.5 times the rated current for a duration of five seconds following the application of a short. The current sense circuit monitors the output of each phase through current transformers. Each transformer output is rectified by diodes to produce an equivalent dc voltage that is fed into the output

overcurrent sense logic circuit for detection of an overcurrent condition. After the five-second duration, the inverter output is cycled off and on until the overcurrent condition is corrected.

i. Major and Minor Drive. The major and minor drive circuits receive the waveform from the drive logic circuit and provides an amplification and buffering of these waveforms for the major and minor bridge converter circuits.

j. Major and Minor Bridge Converters. The major and minor bridge converters receive amplified and buffered waveform signals from the major and minor drive circuits. The waveform signals are converted into quasi sine waveshapes (chopped dc waveforms); one uniquely phased quasi waveshape for the major and another for the minor converter. These quasi sine wave forms are fed into the major (T1) and minor (T2) transformers where they are superimposed upon each other to produce the 3Ø, 115 vac, 400 Hz, sine wave output voltage.

k. Output EMI (Electromagnetic Interference) Filter. The output EMI filter reduces conducted and radiated energy.

k. Output Filter. The filter is tuned to the 12th harmonic; the undesired 11th and 13th harmonics are suppressed from the inverter output voltage.

2-2. Static Inverter Circuit Description

The following circuit description refers to figure FO 2-2, sheets 1, 2 and 3. Circuit paths from one sheet to another are referred to in this discussion as schematic points (⚠ , ⚠ , etc.).

a. High Level Boost. Input voltage from the EMI filter is fed to input chokes L201 and L301 (see fig. FO 2-2, sheet 1) and the center tap of each choke is alternately shorted to ground by a switching circuit (Q206, Q207, Q208, Q306, Q307, Q308). The cycle is: (1) first choke shorted to ground for heavy current flow. (2) first choke removed from ground and stored energy of choke released to heavy duty capacitors, (3) second choke shorted to ground for heavy current flow, (4) second choke removed from ground and stored energy of choke released to heavy duty capacitors, (5) cycle repeated. All during periods (2), (3), and (4), first choke is not shorted to ground and is free to release energy to heavy duty capacitors; each choke then has one period of high current flow where it builds up energy and three periods of releasing the energy to capacitors C401A and C401B. Also, note that every other cycle, (2) and (3), no choke is being shorted to ground. In detail during heavy current flow period, energy will be stored in the choke equal to one-half the inductance times the current squared. The stored energy is alternately released for each choke and discharges through diode CR307 and CR207 to charge capacitors C401A and C401B which creates the 37 vdc supply. Diodes CR307 and CR207 block current flow during energy build up when the voltage across each choke is the opposite of what it will be during choke discharge of energy. Diodes CR306 and CR206 prevent excessive voltage spikes when the chokes are switched from energy charge to discharge. The energy charge (choke center tap effectively shorted to ground) cycle of the chokes is accomplished by utilizing power switch transsistors Q206, Q207, Q208, Q306, Q307 and Q308. These transistors recieve base drive power from current drive transformers T201 and T301.

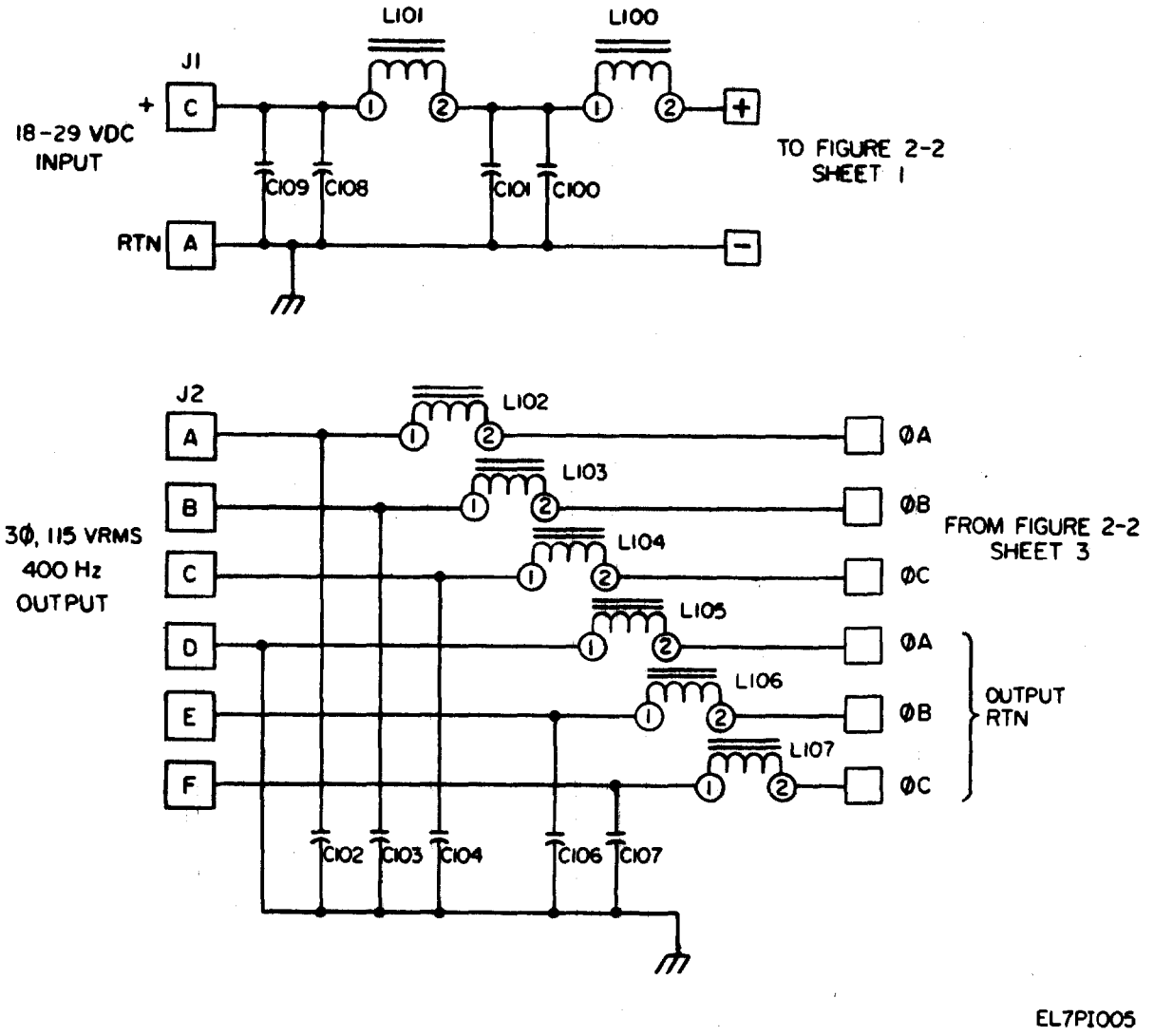


Figure 2-3. Inverter EMI Filter Schematic Diagram.

When transistor Q700 or Q701 is turned on, transformer T201 or T801 secondary winding 4-3 has current flow from the +15 volts through Q700 or Q701 to ground. This resets the respective transformer. Then when transistor Q700 or Q701 is turned off, the energy stored earlier causes a back EMF through secondarywinding 4-3 that flows through diode CR701 or CR702 to ground. This current flow feeds a voltage into primary winding 1-2 of transformer T201 or T301 and supplies the bias voltage which turns on power switch transistors Q206, Q207, Q208, Q306, Q307 and Q308. Thus, choke L201 and L801 have no charge current flow (only discharge current flow) when transistor Q700 and Q701 are turned on but the choke center taps are shorted to ground when Q700 and Q701 are turned off.

The detailed cycling of the boost circuit is: During cycle 1, choke L201 center tap is shorted to ground and choke L301 is unshorted and discharging into capacitors C401A and B. During cycle 2, choke L201 and L301 are unshorted and discharging into capacitors. During cycle 3, choke L301 center tap is shorted to ground and choke L201 is unshorted and discharging into capacitors. During cycle 4, chokes L201 and L301 are unshorted and discharging into

capacitors, etc. In detail, when the nominal +37 V at capacitors C401A and C401B reaches a low limit it is sensed and corrected as follows. The low voltage output at capacitor C401A and C401B goes across resistor divider network R731, R732, R733 and R734. This voltage is compared with zener diode CR707 reference voltage by comparator Z703-B. The output of comparator Z703-B is positive and goes to input pin 5 of comparator Z703-C and when it is a higher positive amplitude than the positive amplitude from capacitor C705 at input pin 4 of Z703-C (to be explained below), then Z703-C output is high. This high will set comparator Z703-D output to high which results in the following:

- 2701 nand gate input pine 1 and 2 are high causing a low at output pin 3 which sets flip-flop Z702 output pins 12 and 13 to the opposite states (i.e., if pin 12 was high and pin 13 low, then pin 12 is now low and pin 13 high). This causes Z700 nand gate output pins 3, 6 and 8, 11 to switch to opposite states so that transisitors Q701 and Q700 now go to opposite states from the lst cycle in which one of them conducted. Note that in the cycle just before this, when comparator Z703-D was low, both transistors Q701 and Q700 were turned on causing both chokes L301 and L201 to lose their center tap ground path through the power switch transistors. If in this case transistor Q700 base was at low from Z700 nand gate output pins 3 and 6, then transistor Q700 would be turned off and transformer T201 secondary winding 5-6 would generate bias voltage in primary winding 1-2 and turn-on power switch trnsistors Q206 through Q208. This would cause heavy current flow in choke L201. At the same time transistor Q701 would be turned on by a high at its base, which would result in current flow through secondary winding 4-3 of transformer T801. This would continue the turned off condition of transistors Q306 through Q308 and choke L301 center tap would not be Shorted to ground; L601 would be discharging any remaining energy into capacitors C401A and C401B.
- The high at comparator Z70-D output also causes a high at Z701-8 nand gate output (pin 8) which turns on transistor Q704 for the short RC time needed to charge up capacitor C704. The momentary turn-on of transistor Q704, discharges the positive voltage on capacitor C705 but, as stated above, transistor Q700 (for example) will now be turned off thus allowing the +15 volt supply current through transformer T201 winding 3-6 to diode CR705A to charge charge up capacitor C705 again. When the charge reaches a high level, the positive voltage at camparator Z703-C input pin 4 overrides the input at pin 5 and sets comparator Z703-C output to low. In addition, the total amount of choke L201 current flow through transformer T201 winding 7-8 also effects the charge-up of capacitor C705. The more current flow, the more voltage induced into the secondary of T201 which adds to the voltage sent to capacitor C705 thus the less time choke L201 center tap is shorted to ground. Note that during the time needed to charge capacitor C705, choke L201 center tap is being shorted to ground and the choke is storing up energy to later be fed to capacitors C401A and C401B for the +37 vdc supply. This low established at comparator Z703-C output will cause a low at comparator Z703-D output which in turn will cause all power switch transistors Q206, Q207, Q208, Q306, Q307 and Q308 to be turned off (described in detail below) thus removing the center tap of both chokes L201 and L301 from ground. Therefore, chokes L201 will no longer store energy but will discharge energy; and also, the logic will now be set so that the opposite choke L301 will be the next to store energy during the next storage cycle. After each choke L201 or L301 has stored up a given amount of energy, the low at comparator Z703-C output will occur and stop the charging up of that choke. The capacitor C705 charging circuit in general will provide that when the 37 vdc is low, choke L201 or L301 will be shorted to ground (to store energy) for a short time and then, after a total discharge cycle, the other Choke via flip-flop Z702) will be shorted; thus establishing a push-pull operation.

In the case when the +37 volt capacitors C401A and C401B are not low and are at the proper +37 volts, then the voltage at comparator Z703-B input pin 10 is high with respect to zener diode CR707 reference input pin 11. The high at pin 10 will set comparator Z703-B output to low which sets comparator Z703-C output low which sets comparator Z703-D output low. This has the following results.

- Nand gate Z701 input pins 1 and 2 are low causing a high at output pin 3 which has no effect on flip-flop Z702 outputs but prepares the flip-flop to be switched at the next low from Z701, pin 3.
- The low at comparator Z709-D output sets nand gate Z700 input pins 2, 5, 10 and 13 to low which sets outpins 3, 6, 8, and 11 to high. This high turns on both transistors Q700 and

Q701 which as described above, sends current from the 15 volts through transformers T201 and T301 causing power switch transistors Q206, Q207, Q208, Q306, Q307, Q308 to be turned off and thus chokes L201 and L301 are not being shorted to ground. This is the only portion of the cycle of operation that both chokes are in the discharge mode. In the next cycle of operation the opposite choke will be shorted to ground.

- The low at comparator Z703-D output also sets nand gate Z701 output pin 8 to low which discharges capacitor C704 preparing it be charged up during next cycle.

b. Overvoltage Sense. When the input voltage or the +37 vdc supply of the inverter reaches a high of 44 volts, the inverter is programmed to shut itself down in order to protect components and to limit excess output AC voltage. The overvoltage sense circuit receives the unit input voltage at the anode of diode CR604 (fig. FO 2-2, sheet 2) and the +37 vdc regulated voltage at the anode of diode CR605. The hgher (more positive) of the two voltages will be present at the cathode of diodes CR604 and CR605. When the higher voltage reaches 44 volts than zener diode CR606 will break down causing transisstor Q605 to turn on. The resulting low at the Collector of Q605 has the following effects:

(1) The output of logic nand gate Z603 pins 3, 6 and 8 are set high which causes the minor drive output logic points Z611 pins 2, 6 and 10 to shut off by being held at low.

(2)Nand gate Z608 input pin 2 is set low which Sets nand gate Z608 output pin 6 to low, resulting in nand gate input Z608 pin 9, Z607 pins 12, 9 ,4, 1 and Z 603 pin 12 being set low which causes the major drive output logic Z610 pins 2, 4, 6 and Z609 pins 2, 4, 6 to shut off by being held atlow.

(3) Nand gate input Z608-12 is set low which puts a high at prom Z602-2 chip enable input, thus setting prom output pins 1 though 6 to low, this turns off all major and minor bridge logic outputs.

(4) The low at collector of transistor Q605 at schematic point ⚠ goes into figure FO 2-2, sheet 1, where it disables the +37 vdc boost regulation circuit.

In detail, nand gate Z701 input pin 12 (fig. FO 2-2, sheet 1) is set low causes transistor Q705 to turn on causing a low at comparator Z703-B input pin 11. This low removes the effect of zener diode CR707 and sets Z703-B output low which sets comparator Z703-C output low which sets comparator Z703-D output low which finally turns off all power switch transistors Q206, Q207, Q208, Q306, Q307, and Q308, thus removing the low impedance to ground to the center tap of chokes L201 and L301. This cuts off all high energy charging of chokes L201 and L301 and thus all high energy charging of capacitors C401A and C401B to 37 volts. However, capacitors C401A and C401B are still able to charge up to the level of the inverter input voltage through the path of input chokes L201 and L301 and diodes CR307 and CR207. It is this input voltage level that is used to produce the +15 vdc supply which is still required for the overvoltage sense circuit so that when an overvoltage condition is no longer present, full operation of the inverter will be restored.

c. Overcurrent Sense. AØ, BØ and CØ output current is monitored by current transformers T500 through T502 (fig. FO 2-2, sheet 3). An ac voltage proportional to the current is present at load resistors R500 through R502 and this voltage is rectified by diodes CR500 through CR505 and the dc voltage is sent to the overcurrent sense logic circuit (fig. FO 2-2, sheet 2). The Varying dc voltage is made more smooth through resistor R626 and capacitor C607 and then fed to comparator Z601-5 positive input. An overcurrent condition will cause the Z601-5 input to exceed the zener diode CR603 reference vltage input at comparator Z601-4 negative input. This drives output Z601-2 to high. Comparator Z601-1 output, however, is set to low by an overcurrent condition because the dc error voltage in this case goes to Z601-6 negative input. The low at comparator Z601-1 output goes to prom Z602-14 input and programs the major bridge logic for low voltage and high current rather than the normal quasi sine waveform. The minor bridge is programmed for the quasi sine waveform. The inverter output will now be able to conduct a high level of current for the next 5 seconds until further logic (described below) turns off all major bridge logic outputs⚠ through ⚠.

The overcurrent high at comparator Z601-2 output allows capacitor C606 to charge to a high which triggers timer Z606. This causes timer Z606-4 output to produce a momentary low pulse five seconds after input Z606-10 went high. The momentary low at Z606-4 sets nand gate Z605-6 output to high. This high is at nand gate Z605-2 input and since other input Z606-1 is normally high, then Z605-3 output goes low causing Z605-6 output to latch at high. The latched high goes to nand gate Z605-12 input and since other input Z605-13 is at high due to overcurrent condition, output Z605-11 is set to low. The high-low transition at Z605-11 output triggers timer Z604-1 input which cause a 1.5 second positive ulse at timer output Z604-13 (the negative pulse at timer

output Z604-4 only ensures that latch Z605-6 will remain at high as explained below). The high pulse at Z604-13 goes to nand gate input Z605-10 along with the high at input Z605-9 from the latch. Nand gate output Z605-8 is then set to low by the two highs and this low, finally, causes a low at nand gate output Z608-6 which turns off all inverter output current by setting major bridge logic signals ⚠ through ⚠ to low for 1.5 seconds. The absence of current for 1.5 seconds puts a low at nand gate input Z605-13 which sets timer input Z604-1 to high. After the 1.5 second, when the major bridge logic outputs ⚠ through ⚠ and inverter output current is enabled again, if an overcurrent condition is still present, then nand gate input Z605-13 will go back to high, setting output Z205-11 back to low (other input Z605-12 is still held at high by latch Z605-6). This sequence of high-low at timer input Z604-1 triggers the timer again and another 1.5 second high pulse is sent out at timer output Z604-13. This pulse again shuts off all inverter output current for 1.5 seconds. However, afer the 1.5 seconds, if at this time the overcurrent condition is removed, then nand gate input Z605-13 will remain at low and timer input Z604-1 will not be triggered and thus the inverter output current will not be shut off. The absence of he overcurrent condition also sets comparator output Z601-1 to high Which goes to prom input Z602-14 and restores the prom to program the normal quasi sine waveform at major bridge logic outputs ⚠ through ⚠ ; and also restores normal minor bridge outputs ⚠ through ⚠ . The inverter is now restored to its normal condition except that latch output Z605-6 is still latched at high; if it remained latched then if another overcurrent condition occured then timer Z604-1 input would be triggered at once rather than five seconds after the overcurrent condition. Therefore, the latch is reset as follows. when inverter has no overcurrent condition then timer Z604-1 input is no longer triggered and timer Z604-4 output remains at its normal high level (during overrcurrent condition Z604-4 outputs a low pulse every few seconds); this high level puts a long term high at the cathode of diode CR610. The cathode of diode CR609 is also at high due to the high at nand gate latch Z605-6 output. The two highs allow the normal condition of a high at the base of transistor Q606 which turns it off and causes transistor Q607 to turn off.Capacitor C611 can now charge up in about seven seconds to a high that sets comparator Z601-14 output to low. This low goes to nand gate input Z605-1 which causes a high at latch input Z605-4 which in turn sets latch output Z605-6 to low because latch input Z605-5 is high due to timer Z606 being in its normal, untriggered state. The latch circuit is now ready for the next overcurrent condition. Also, with the low now at latch output Z605-6, the cathode ofCR609 is at low which turns on transistor Q606 and then transistor Q607, which in turn shorts out capacitor C611 setting negative input Z601-8 of comparator at low causing comparator output Z601-14 to go to its normal high level.

d. Inverter Turn-On. When the inverter is initially turned on, protective logic circuits are employed to hold off operation of several sections of the inverter until other sections are operative.

(1) *Protective delay of inverter output voltage and 37 vdc boost voltage for first second after turn-on.* Timer Z604-10 input (see figure FO 2-2, sheet 2) is triggered by a low-high transient due to capacitor C604 charging up to a high from the high level at comparator output Z601-1. Timer output Z604-5 now delivers a on-second high pulse to the anode of diode CR607 causing transistor Q605 to turn on which sets the transistor Q605 to low. This low at schematic point ⚠ to figure FO 2-2, sheet 1, inhibits the 37 vdc boost voltage from turning on (as described above in the case of an overvltage condition) and also goes to rand gate input Z-608-12 to put a high at vrom Z602-15 chip enable input which holds all major and minor bridge logic outputs (schematic points ⚠ through ⚠) at low so that inverter output voltage is cut off. The low at collector of transistor Q605 also directly holds major bridge logic output schematic points ⚠ through ⚠ at low and minor bridge logic output schematic points ⚠ , ⚠ , and ⚠ at low by controlling the nine associated nand gates. This delay is inverter output voltage allows the 9.6 kHz oscillator counter and prom circuits time to stabilize. Also, note that the inverter 37 vdc supply can still build up enough power to supply energy to the +15, vdc supply even though the 37 vdc boost regulation circuit has been temporarily held off.

(2) *Protective delay of +5 vdc supply, inverter output voltage and 37 V boost voltage until +15 vc supply has reached a minimum of 13 volts.* Immediately after turn-on of inverter before +15 vdc supply has reached 13 Volts, comparator positive input Z601-11 which sees the +15 volt supply will be low in relation to input pin 10 zener diode CR603 reference, and Z601-13 output will thus be low. This low turns on transistor Q604 puttin a high at the anode of CR68 which turns on transistor Q605, resulting in a low at collector of transistor Q605. This low holds off inverter output power through logic outputs ⚠ through ⚠ (as described above) and also holds off turn-on of 37 volt boost regulator through low signal at schematic point ⚠ which goes to boost circuit (as described

above). In addition, the original low at the collector of Q604 also causes turn-off of transistor Q608 putting a low at collector of transistor Q608. this low at schematic point goes to figure FO 2-2, sheet 3, where it turns off transistors Q50 and Q505 thus holding off the +5 vdc supply until the +15 vdc supply has reached at least 13 volts. Another end result of transistor Q608 turning on until the +15 vdc supply is proper is that the low at collector of transistor Q608 goes through diode CR612 add resets the latch circuit by setting nand gate output Z605-5 to high which sets latch output Z605-6 to low; thus preparing circuit for detection of possible overcurrent condition.

e. Drive Logic.

(1) *9.6 kHz oscillator.* The drive logic is controlled by a 9.6 kHz oscillator (fig. FO 2-2, sheet 2) consisting of transistors Q600 through Q603 and associated components. Initially, tranistor Q600 will be turned off and the remaining transistors will be turned on. With transistor Q602 conducting, a positive voltage will be coupled through diode CR601 and through set-in test resistors R60 and R607 to charge up capacitor C601. The charge on capacitor C601 turns on transistor Q600 which causes transistor Q601 emitter to be more positive than its base which turns off transistor Q601. This in turn puts a high at the base of transistor Q602 and turns it off. Transistor Q603 is not turned off and its collector potential goes high. At the same time the charge voltage for capacitor C601 is no longer at the anode of diode CR601 and the capacitor will start to discharge through resistors R607, R608 and R609. The discharge will continue until transistor Q600 is turned off and the cycle repeats itself producing a 9.6 kHz square wave at the collector of transistor Q603. The square wave is divided and programmed by counter Z600 and prom Z602 to produce the logic gating (at schematic points ⚠ through ⚠) pulses for the major and minor bridges.

(2) *Output logic drive signals.* The 9.6 kHz square ave is fed counter Z600 and from there to prom Z602. The orignal 9.6 kHz wave is counted down and converted into the logic drivo signals for the major bridge, which exits A6 logic board at schematic points ⚠ through ⚠ (see below for waveform), and *the logic drive* signals for the minor bridge, which exits the A6 logic board at schematic points ⚠through ⚠For the major bridge signals, the three outposts of prom Z602-1, -2, -3 are fed to nand gates Z603-13, Z607-5 and Z607-13 where each signal is given a second, inverted, output line through nand gate Z607-2, Z607-10 and Z608-10. The six logic signals are amplified and buffered by six inverting amplifiers Z610 and six inverting amplifiers Z609 and the final six logic outputs go to A4A1 board (fig. FO 2-2, sheet 3) through schematic points ⚠ through ⚠ .For the minor bridge signals, the three outputs of prom Z602-4, -5, -6 are fed to nand gates Z603-1, Z603-4 and Z603-9 and also directly to inverter amplifiers Z611-3, Z611-9 and Z811-13 for an inverted output. All six logic signals are amplified and buffered by inverting amplifiers; three by the original inverting amplifiers Z611-3, Z611-9 and Z611-13 and the other three by inverting amplifiers Z611-1, Z611-5 and Z611-11. Note that in the case of an output overcurrent condition, prom Z602 is programmmed for the first five seconds by a low at input pin 14 to cause a special waveform output at output pins 1 through 6 so that the inverter output goes to low voltage and accepts high current flow. In the case of an input or 37 vdc supply overvoltage condition or during initial turnon, prom ZZ602 pin 15 chip enable input is turned off by a high and, thus, all major and minor bridge logic signals are set to low, turning off the inverter output.

f. Major and Minor Drive and Bridge Converter, The major bridge consists of transistors Q200 through Q205 and diodes CR200 through CR205 (fig. FO 2-2, sheet 3). The minor bridge consists of transistors Q300 through Q305 and diodes CR300 through CR305. Both circuits function in a similar manner with the exception of timing an power-level differences. Schematic points ⚠ through ⚠ are the inputs from the logic circuits that control the major drive section and points ⚠ through ⚠ are the inputs from the logic circuits that control the minor drive section. The major and minor sections perform the same in theory, the difference being in the power levels and gating sequence. The major and minor sections are divided into three identical divisions to produce phase A, phase B and phase C output voltage. However, due to the relationship of the logic signals the individual phases can only be isolated at the output transformers T1 and T2. The input signals at points ⚠ and ⚠ are 180 degrees out of phase, likewise, Points ⚠ to ⚠ , ⚠ to⚠ , ⚠ to⚠ ,⚠ to ⚠ and⚠ to⚠ This allows only one control transistor to conduct at a time which permits current control in the associated transformer. The current control produces polarity changes in the secondary, which gates associated transistors, which then determines whether the output transformer has current flowing or not and if so in what direction. The waveshapes shown in figure 2-4 represent the inputs from the logic circuits to the major drive section.

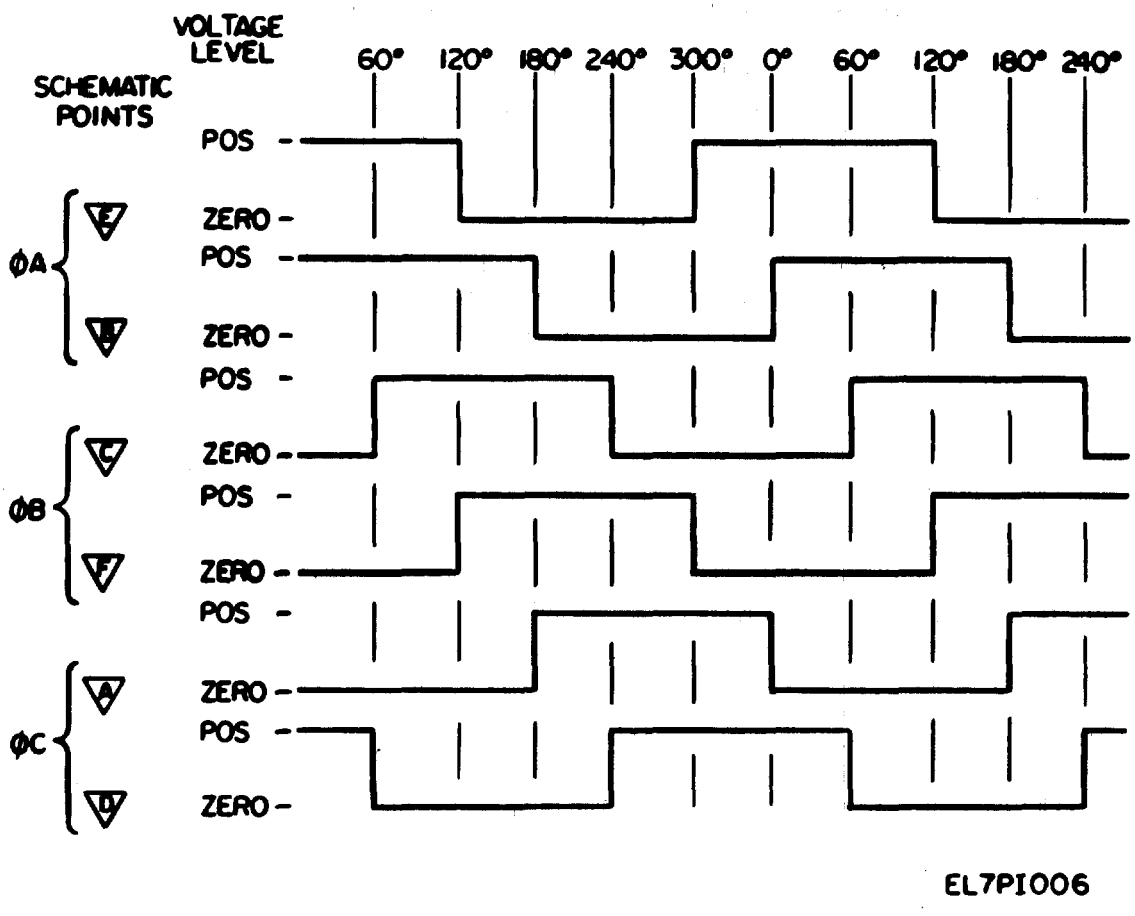


figure 2-4. Waveshape Inputs from Logic Cicuits to Major Drive Section.

The waveshapes at points ▲ and ▲ are used to produce the composite waveshape for phase ▲ (points ▲ and ▲ produce Phase B, points ▲ and ▲ produce phase C). When the logic level of point E is positive, transistor Q404 will conduct through transformer T402 in such a direction that the polarity dots will be positive. This positive will forward bias transistor Q205. At the same time the logic level of point ▲ is positive causing transistor Q401 to conduct through transformer T400 in such a direction that the ends opposite the polarity dots will be positive. This positive will forward bias transistor Q200. We now have a complete circuit for current to flow through transistor Q205, through primary winding (phase A) of transformer T1, through transistor Q200 to ground. This condition will last for 120 degrees of a 360 degree cycle. During this 120 degree period the waveshape at point went positive causing transistor Q402 to conduct through transformer. T401 in such a direction that the polarity dots will be positive. This positive will forward bias transistor Q203. At the end of 120 degrees point ▲ goes to zero and point ▲ goes Postive. Transistor Q405will now conduct reversing the direction of current flow in transformer T402 causing Transistor Q205 to cut off and transistor Q31 to conduct. When transistor Q204 conducts a circuit is completed through primary winding (phase B) of transformer T1, through transistor Q203 (turned on previously) to the 37 vdc power source. This condition will last for an additional 60 degrees (total 180 degrees at which time point ▲ goes to zero and point ▲ goes positive causing transistor Q401 to conduct and transistor Q400 to cut off which will reverse direction of current flow in transformer T400. Transistor Q201 will conduct and transistor Q200 will cut off. transistor Q201 will provide 37 vdc through primary winding (phase A) of transformer T1 (opposite direction from previous current flow). By continuing the above process a quasi waveshape will be produced for each of the three phases as shown in figure 2-5.

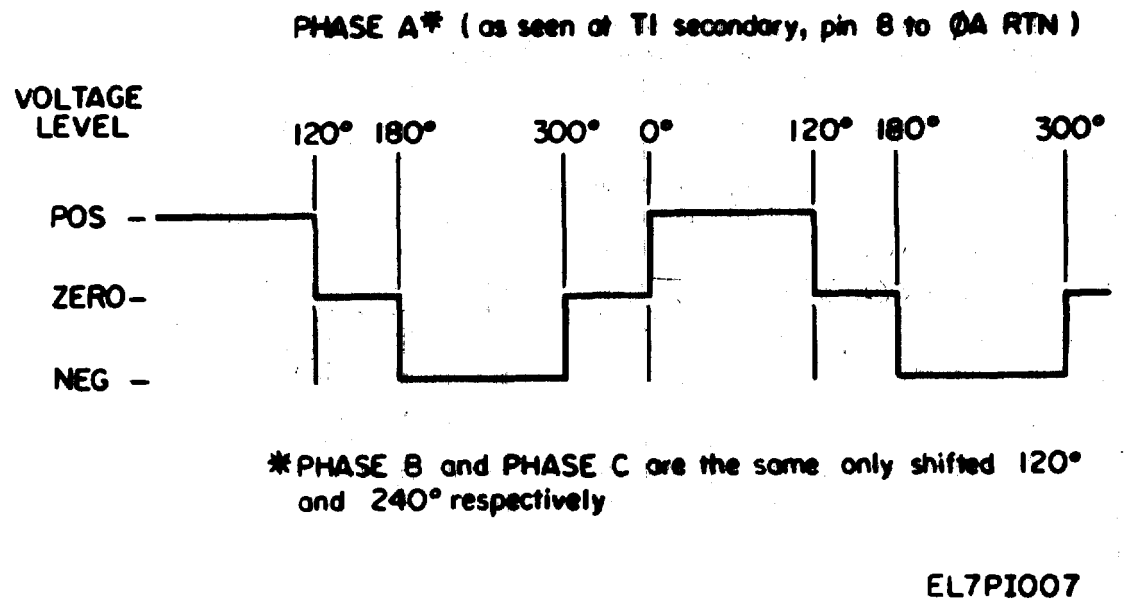


Figure 2-5. Quasi Waveshape for Each Phase.

The waveshapes shown in figure 2-6 represent the inputs from the logic circuits to the minor drive section. The waveshapes at points ⚠ and ⚠ are used to produce the composite waveshape for phase A (points ⚠ and ⚠ produce phase B and points ⚠ and ⚠ produce phase C).

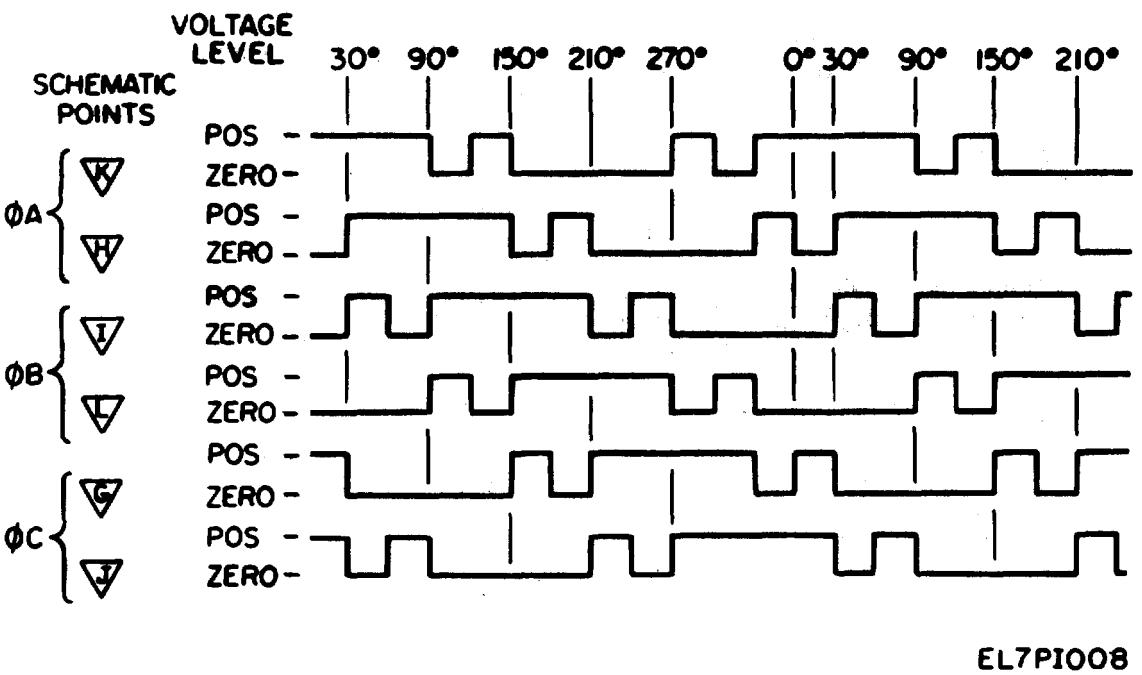


Figure 2-6. Waveshape Inputs from Logic Circuits to Minor Drive Section.

When the logic level of point A is positive, transistor Q41O will conduct throuh transformer T405 in such a direction that the polarity dots will be positive. This positive will forward bias transistor Q305. At the same tme the logic level of point A is positive (point A is negative) causing transistor Q406 to conduct through transformer T409 in such a direction that the polarity dots will be positive. This positive will forward bias transistor Q3O1 applying 37 vdc to both sides of primary winding (phase A) of transformer T2 (current flow static). This condition will last for 30 degrees of a 360 degree cycle. Then the logic level at point A and A will switch causing transistor Q407 to conduct (Q406 will cut off) through transformer T403 in such a direction that the ends opposite the polarity dots will be positive. This positive will forward bias transistor Q300. This completes the circuit for current to flow through transistor Q305, through primary winding (phase A) of transformer T2, through transistor Q300 to ground. These Conditions remain unchanged for a duration of 60 degrees at which time point A goes negative (point A goes positive) applying ground to both sides of primary winding phase A of transformer T2 current flow static). This condition will last for 30 degrees at which time point A again goes positive and current flow is resumed. This condition will prevail for an additional 30 degrees at which time both points A and A change logic levels causing the current flow to reverse direction. By continuing the above process a quasi waveshape as shown in figure 2-7 will be produced.

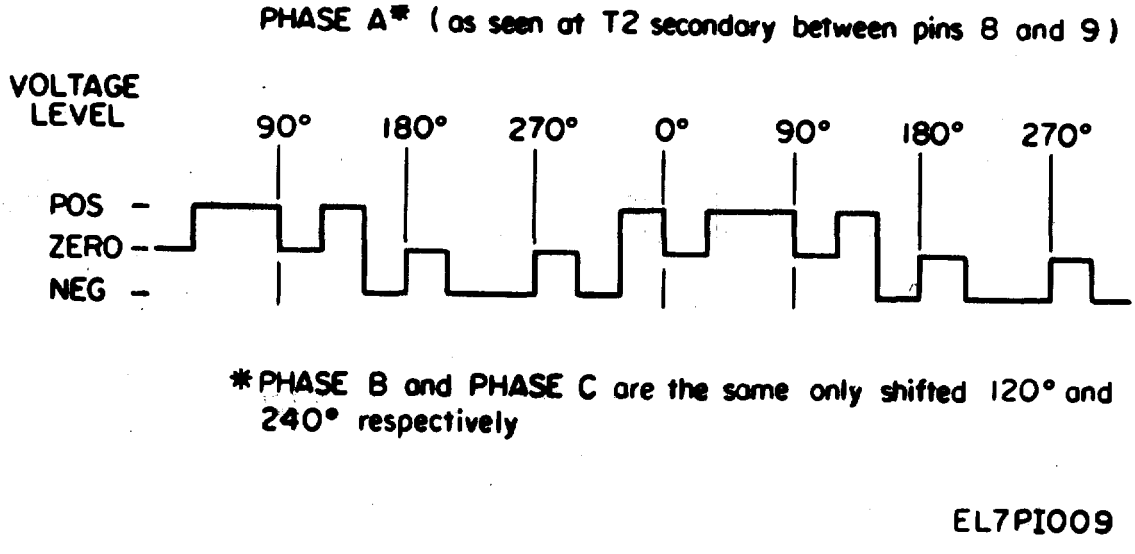


Figure 2-7. Minor Composite Waveshape.

The major and minor composite waveshaes are superimposed and after filtering by the chokes and capacitors, they produce the 115 vrms output sine wave.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section 1. GENERAL

3-1. Voltage Measurements

Table 3-1 lists the voltages that can be expected in the inverter. Perform the instructions in this paragraph only when necessary to check these standard voltages.

WARNING

High voltages and currents are present on disassembled inverter when it is energized. Do not touch any exposed wiring or any metal point within the inverter: Lethal shock could result.

a. Partially disassemble inverter (para 3-0 *a* and *b.)* gains access to A1, A4 and A5 modules (6 and 34, fig. 3-21) and A7 component assembly (17).

b. Loosen A7 component assembly (17) by removing six screws (20), six lockwashers (21) and six flat washers (22).

c. Place inverter on work bench with front side down.

CAUTION

When performing **d** below, make sure component, pine and printed wiring on A7 component assembly (17) do not touch chassis ground; do not damage interconnecting wiring.

d. Carefully lay back upper end of A7 component assembly (17) 90 degrees over onto work bench. Avoid strain on interconnecting wiring. A6 component assembly (16) is now accessible.

e. Connect inverter to test fixture as shown in figure 3-1. On test fixture, set load switches S2, S12 and S22 to up position (83.3 VA).

f. Set UNIT PWR switch S6 to ON position and apply 28± 1 vdc input power to inverter.

g. Using Digital Voltmeter AN/GSM-64 (digital voltmeter), measure the voltages as prescribed in table 3-1 at the given pins. See figure 3-10, 8-13, 3-15, 3-17 and 3-18 for location of referenced pins.

Table 9-1 Voltage Measurement

ASSEMBLY	FROM PIN	TO PIN	VOLTS DC	REMARKS
A1, EMI Module	1(+)	10(-)	27 to 29	
A4, Power Caps and Drive	5(+)	6(-)	37 to 41	
A5, Output	13(+)	14(-)	23.0 to 27.0	
Filter and	12(+)	14(-)	13.99 to 14.01	
Bias Regulator	2(+)	14(-)	4.5 to 4.9	
	1(+)	7(-)	4.5 to 5.5	
	5(+)	7(-)	14.5 to 15.5	
A6, Logic	6(+)	7(-)	4.3 to 4.7	With ØA output overloaded, see Note 1.
	6(+)	7(-)	9.8 to 10.2	With ØA output short-circuited, see Note 2.
	TP1(+)	7(-)	3.995 to 4.005	
A7, Component Assembly, Boost	1 +)	4(-)	14.5 to 15.5	
Regulator	5(+)	4(-)	4.5 to 5.5	

Note1. This overload condition is obtained by setting switches S1, S2, S3, S4 and S5 (see fig. 3-1) to the up position. Return switches to down position after taking measurement.

Note 2. This short circuit condition in obtained by setting switch S10 (see fig. 3-1) to SHORT position. Return switch S10 to down position after taking measurement.

h. After completing voltage measurements, set UNIT PWR switch S6 to down (off) position. Disconnect inverter from test fixture.

i If required at this time, carefully lay A7 component assembly (17) back in place on top of A6 assembly (16); be careful of interconnecting wiring. Install A7 assembly with six screws (20), six lockwashers (21) and six flat washers (22).

j. Reassemble top and bottom covers (para 3-10 *m* and *n),* if required at this time.

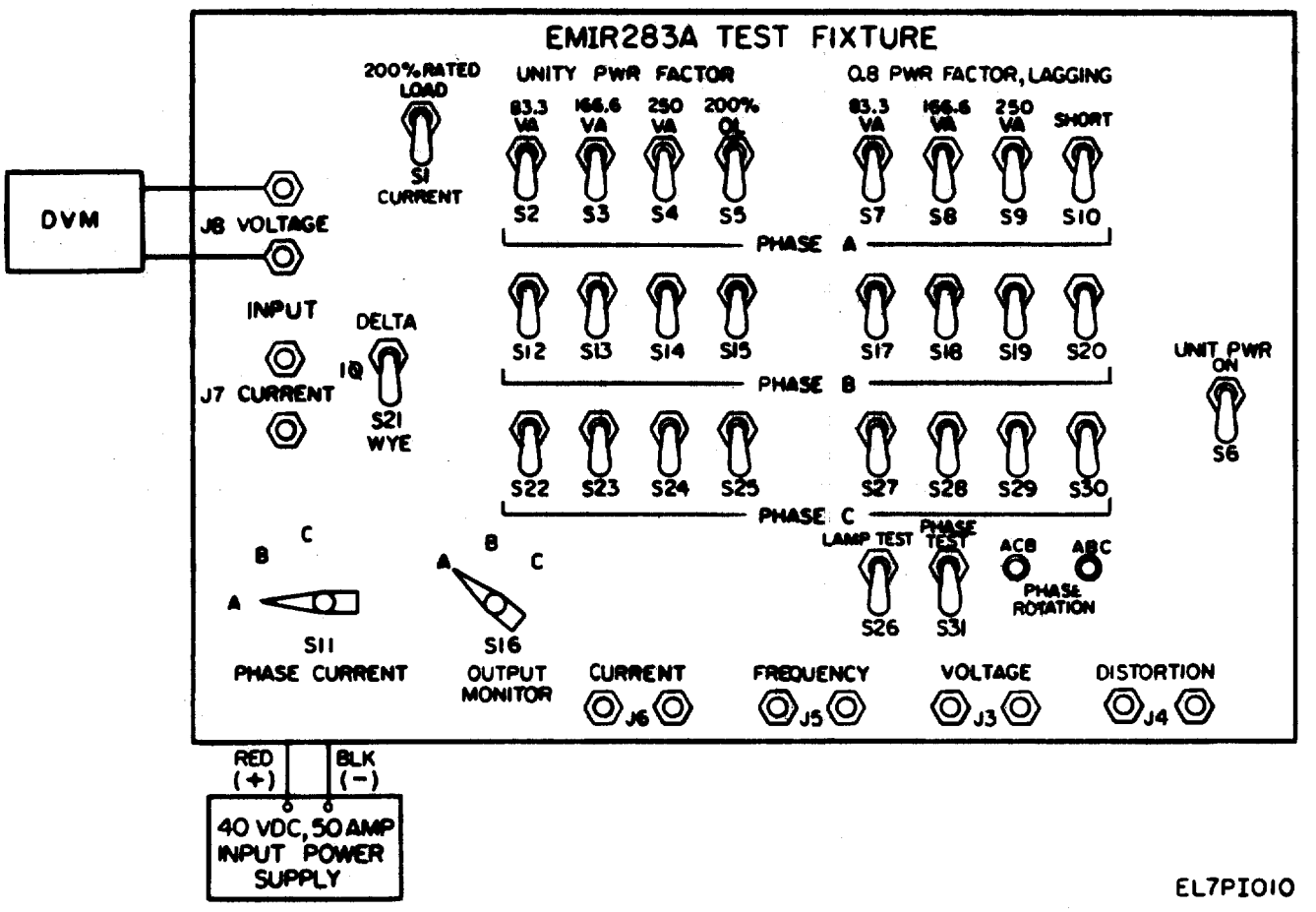


Figure 3-1. Initial Test Setup.

3-2. Waveform Check of Component Assembly A6

The instructions in this paragraph are performed only if internal inverter waveforms are required to be checked on component assembly A6.

WARNING

High voltages and currents are present on disassembled inverter when it is energized. Do not touch any exposed wiring or any metal point within the inverter: Lethal shock could result.

a. Partially disassemble inverter (para 3-9 *a).* This gains access to A7 component assembly (17).

b. Loosen A7 component assembly (17) by removing six screws (20), six lockwashers (21) and six flat Washers (22).

c. Place inverter on work bench with front side down.

d. Carefully lay back upper end of A7 component assembly (17) 90 degrees over onto work bench. Avoid strain on interconnecting wiring and be sure metal pins and connections do not touch inverter case. A6 component assembly is now accessible. See figure 3-17 for location of reference pins.

e. Connect inverter to test fixture as shown in figure-3-l.

f. On test fixture, set load switches S2, S12 and S22 to up (83.3 VA) position. Set UNIT PWR switch S6 to ON position and apply 28±1 vdc input power to inverter.

g. Connect Oscilloscope AN/USM-281 (oscilloscope) and Counter AN/USM-207 (counter) to pins 14(+) and 16(-) of component assembly A6. The observed waveform shall be as shown in figure 3-2 and the counter shall indicate a frequency

between 393 and 407 Hz.

h. Connect the oscilloscope and counter to pins 13(+) and 15(-) of Component assembly A6. The observed waveform shall be as shown in figure 3-3 and the counter shall indicate a frequency between 393 and 407 Hz.

i. Connect the oscilloscope to pins 11(+) and 8(-), pins 10(+) and 9(-) or 18(+) and 19(-) of component assembly A6. The observed waveform shall be as shown in figure 3-3.

j. Connect the oscilloscope to pins 15(+) and 7(–) of component assembly A6. The observed waveform shall be as shown in figure 3-2, except the amplitude shall be approximately 5 volts.

(1) Set ØA switches, S1, S2, S3 and S4 to up (on) position.

(2) Set ØA switch S5 to up (200% OL) position and observe that above waveform goes to 0 volts in 5 to 15 seconds. Observe that within 1 to 1.5 seconds after waveform goes to 0 volts, it returns to normal and then cycles off and on at about a one-second rate.

(3) Set ØA switches Sl and S5 to down position.

k. Connect the oscilloscope to pins ll(+) and 7(-) of component assembly A6. The observed waveform shall be as shown in figure 3-3, except the amplitude shall be approximately 5 volts.

(1) Set ØA switch S10 to up (SHORT) position and observe that above waveform shall convert to a square wave with a frequency between 393 and 407 Hz.

(2) Set ØA switch S10 to down position and observe that waveform drops to 0 volts and returns to level of figure 3-3.

l. Set UNIT PWR switch S6 to down position. Connect the oscilloscope to pins 15(+) and 7(–) of assembly A6. Set UNIT PWR switch S6 to up (ON) position and observe that waveform shall be 0 volts for approximately 1 second before displaying a 400 Hz square wave.

m. Set UNIT PWR switch S6 to down position. Disconnect inverter from test fixture.

n. If required at this time, carefully lay A7 component assembly (17) back in place on top of A6 assembly (16); be careful of interconnecting wiring. Install A7 assembly with six screws (20), six lockwashers (21) and six flat washers (22).

o. Reassemble bottom cover in accordance with para 3-10 *m*, if required at this time.

3-3. Waveform Checks of A5Al, A4A1, A2, A3, A4 and A5 Component Assemblies and Modules

The instructions in this paragraph are performed only if internal inverter waveforms are required to be checked on A5A1, A4A1, A2, A3, A4 and A5 component assemblies and modules. See figures 3-11 through 3-16, as applicable, for location of referenced pins.

WARNING

High Voltage and currents are present on disassembled inverter when it is energized. Do not touch any exposed wiring or any metal point within the inverter. Lethal shock could result.

a. Remove top cover in accordance with para 3-9 *b*.

h. Disconnect wire at pin 13 of component assembly A5A1 and connect a 30 vdc power supply to pins 12(+) and 14(–) of component assembly A5A1. Adjust power supply voltage to 25.0 ±2.O vdc.

C. Connect Oscilloscope AN/USM-281 to pins 10 and 11, 12 and 13 and 14 and 15 of component assembly A4A1. At each connection the observed waveform shall be as shown in figure 3-4.

d. Connect the oscilloscope to pins 16 and 17, 18 and 19 and 20 and 21 of component assembly A4A1. At each connection the observed waveform shall be as shown in figure 3-5.

e. Connect the oscilloscope to pin 4 and Q207-E of module A2. The observed waveform shall be as shown in figure 3-6.

f. Connect the oscilloscope to pin 4 and Q307-E of module A3. The observed waveform shall be as shown in figure 3-6.

g. Connect a 40 vdc, 5 amperes power supply to pins l(–) and 5(+) of module A4. Adjust power supply voltage to 10.0 –0.5 vdc.

h. Connect the oscilloscope to pins 1 and 2, 4 and 7 and 8 and 9 of component assembly A4A1. At each connection the observed waveform shall be as shown in figure 3-7.

i. Connect the oscilloscope to pins 22 and 23, 25 and 28 and 29 and 30 of component assembly A4A1. At each connection the observed waveform shall be as shown in figure 3-8.

j. Increase 40 vdc power supply voltge to 37.0 ±0.5 vdc and repeat *i* above. The observed waveform shall be as shown in figure 3-8 except the peak-to-peak voltage shall be approximately 74 vdc.

k. Increase 40 vdc power supply voltage to 39.0 ±0.5 vdc. Using a X10 probe, connect oscilloscope to pins 22 and 25, 23 and 26, and 24 and 27 of module A5. The observed waveform shall be as shown in figure 3-9.

l. Turn off and disconnect 40 vdc power supply. Reduce the 28 vdc input voltage to 0. Turn off and disconnect the 30 vdc power supply.

m. Solder wire back to pin 13 of component assembly A5A1.

n. Reassemble top cover in accordance with para 3-10 *n*.

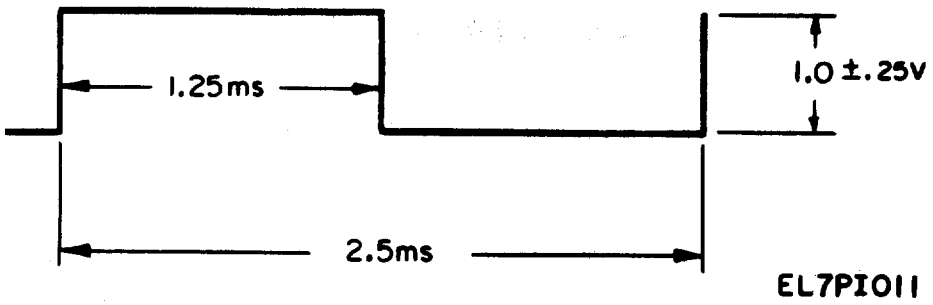


Figure 3-2. Input to Drivers of Major Bridge from Logic Assembly.

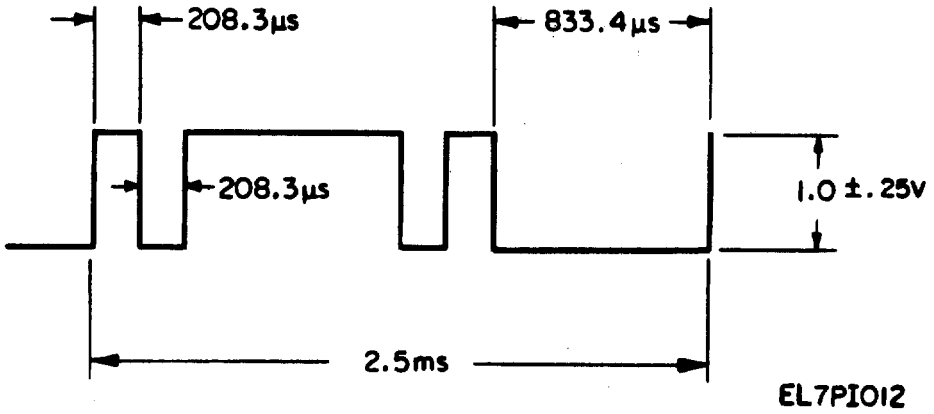


Figure 3-3. Input to Drivers of Minor Bridge from Logic Assembly.

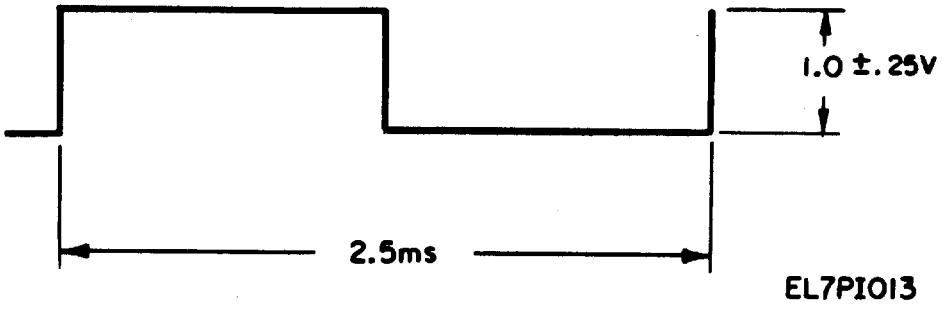


Figure 3-4. Major Bridge Drive Signal.

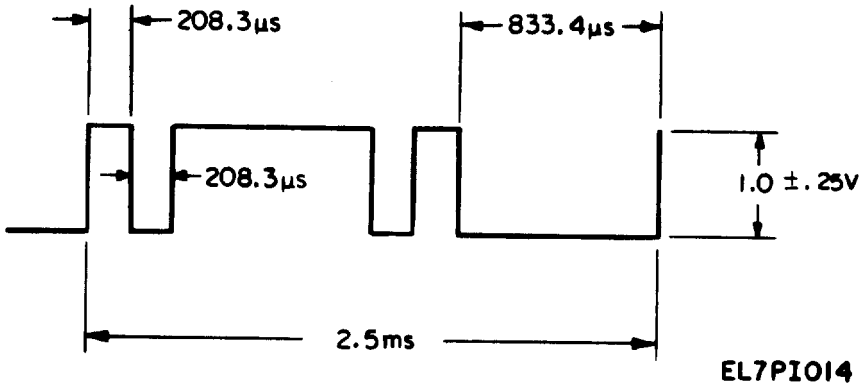


Figure 3-5. Minor Bridge Drive signal

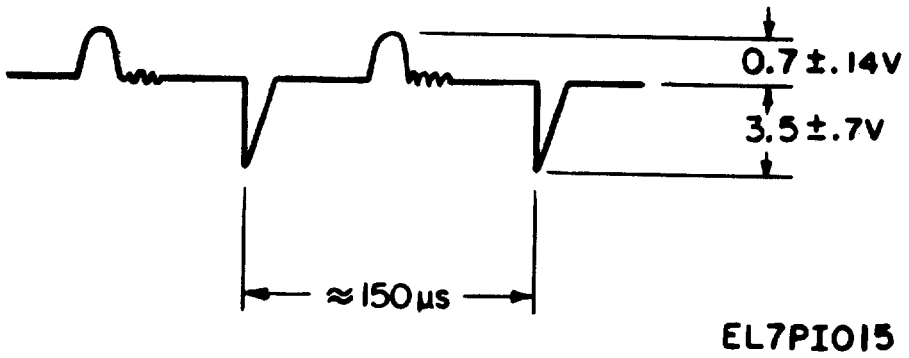


Figure 3-6. High level Boost output.

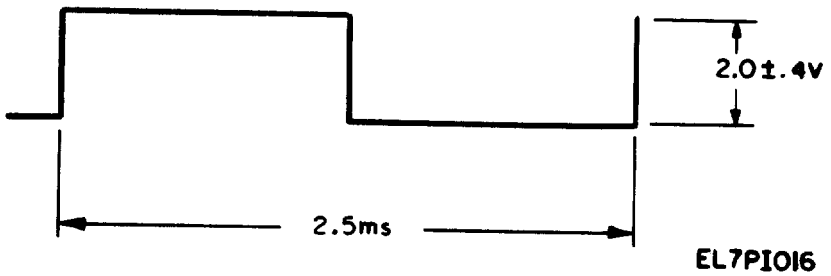


Figure 3-7. Major Bidge Drive Output.

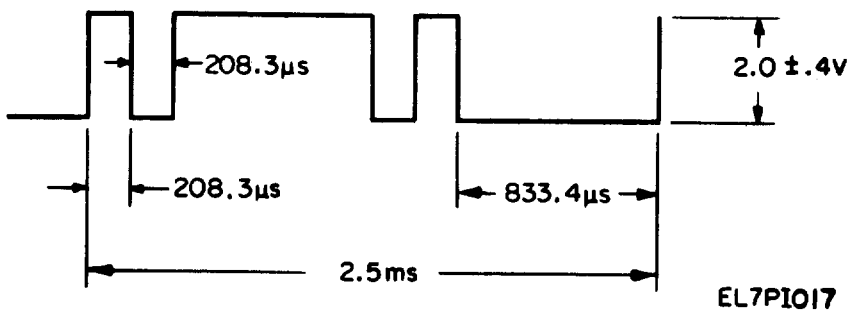


Figure 3-8. Minor Brige Drive Output.

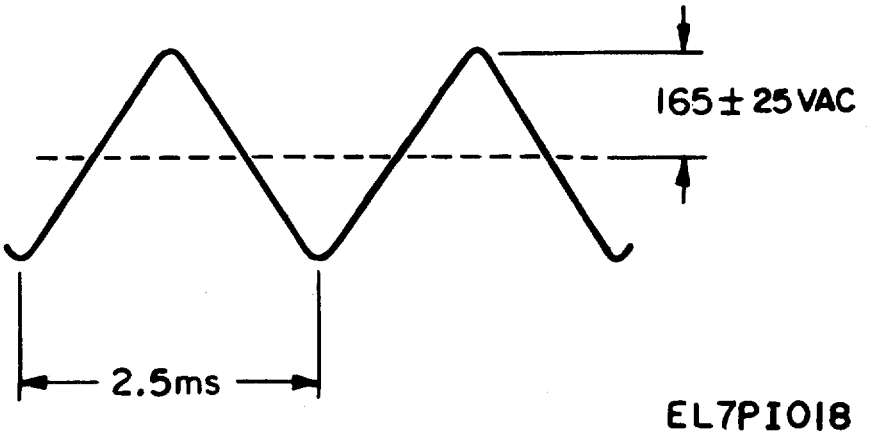
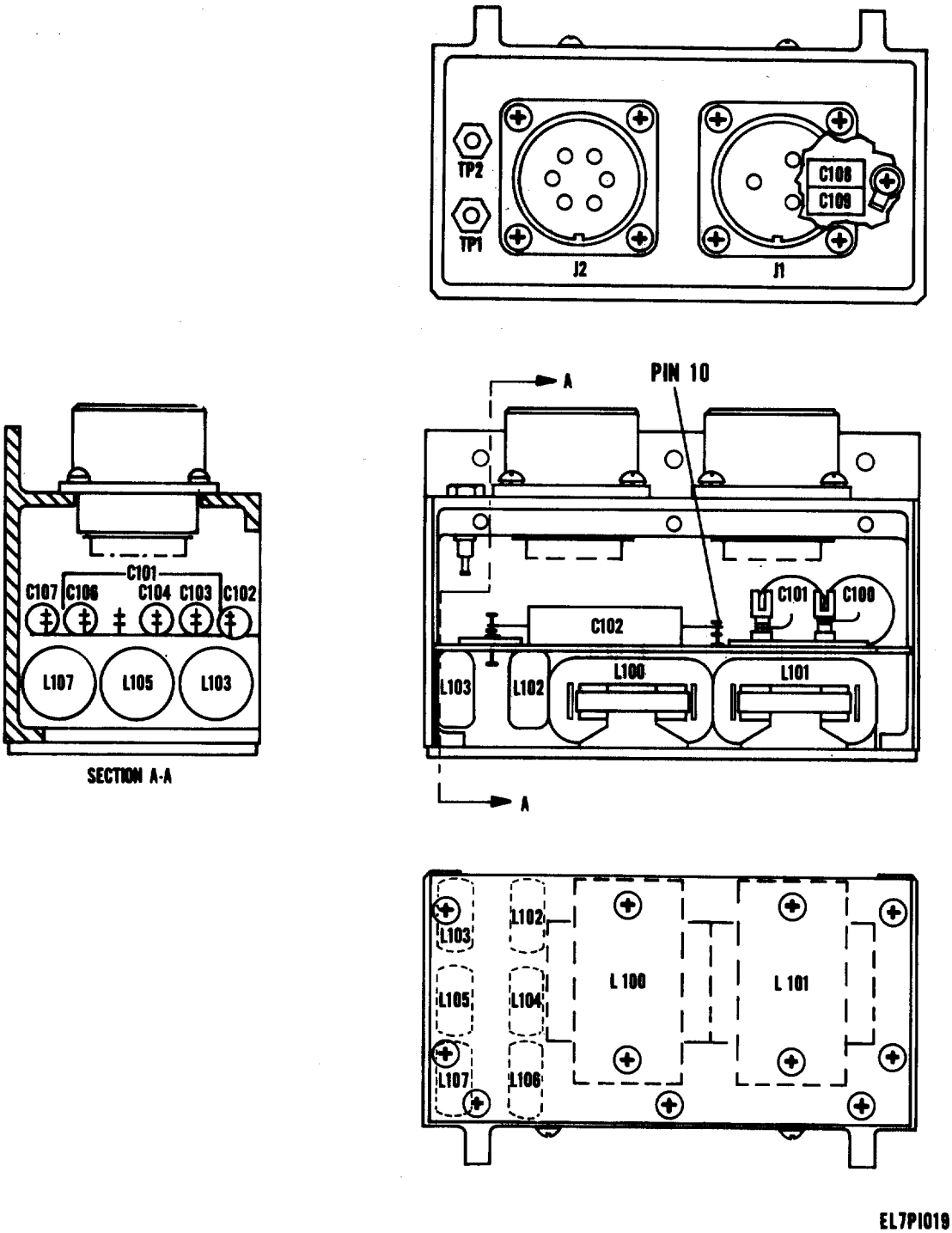


Figure 3-9. Output EMI Filter Output.

3-4. supporting Illustrations

The illustrations of the inverter assemblies referenced in this manual are presented herein as information required for direct support maintenance.



Fgure 3-10. EMI Module A1.

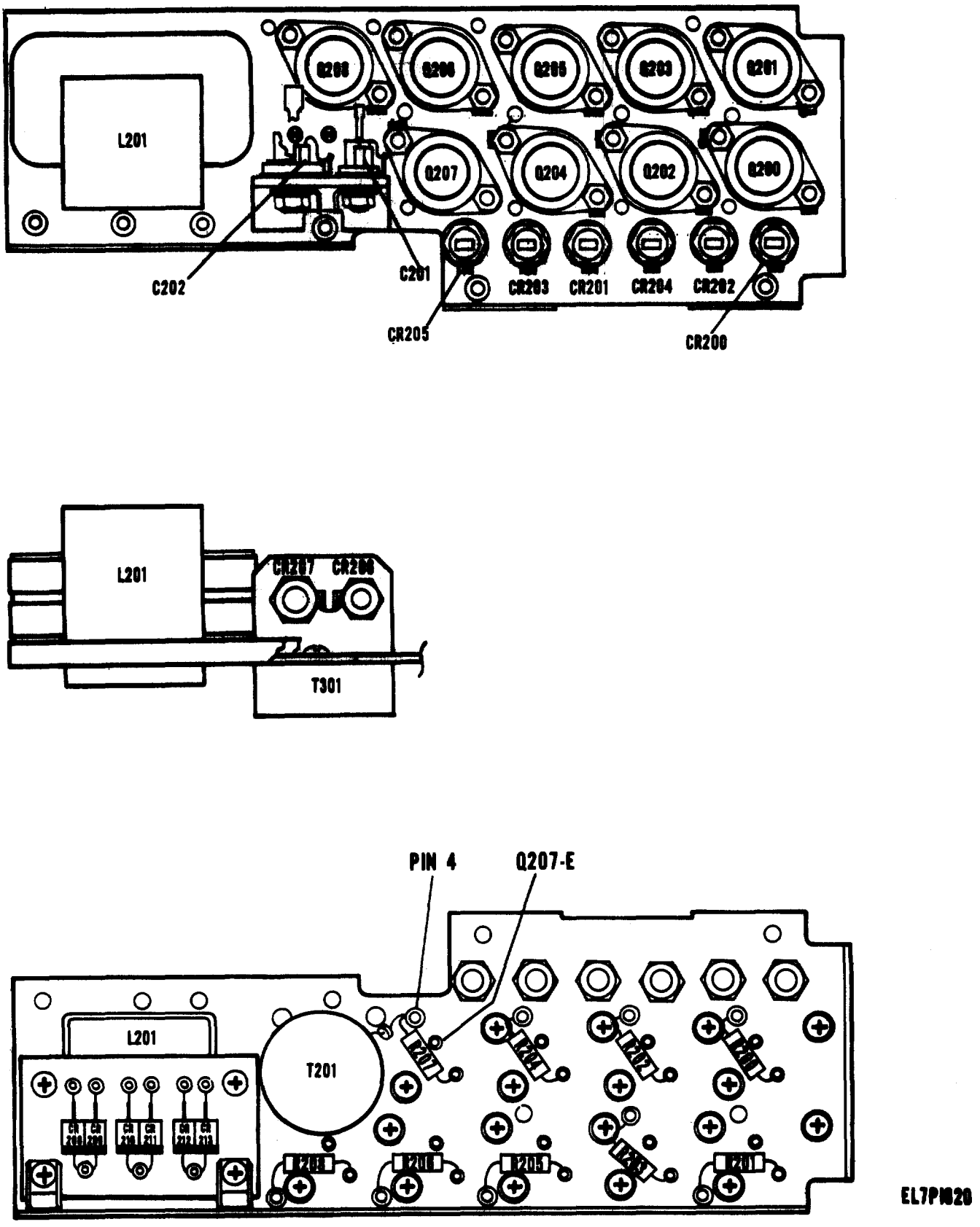
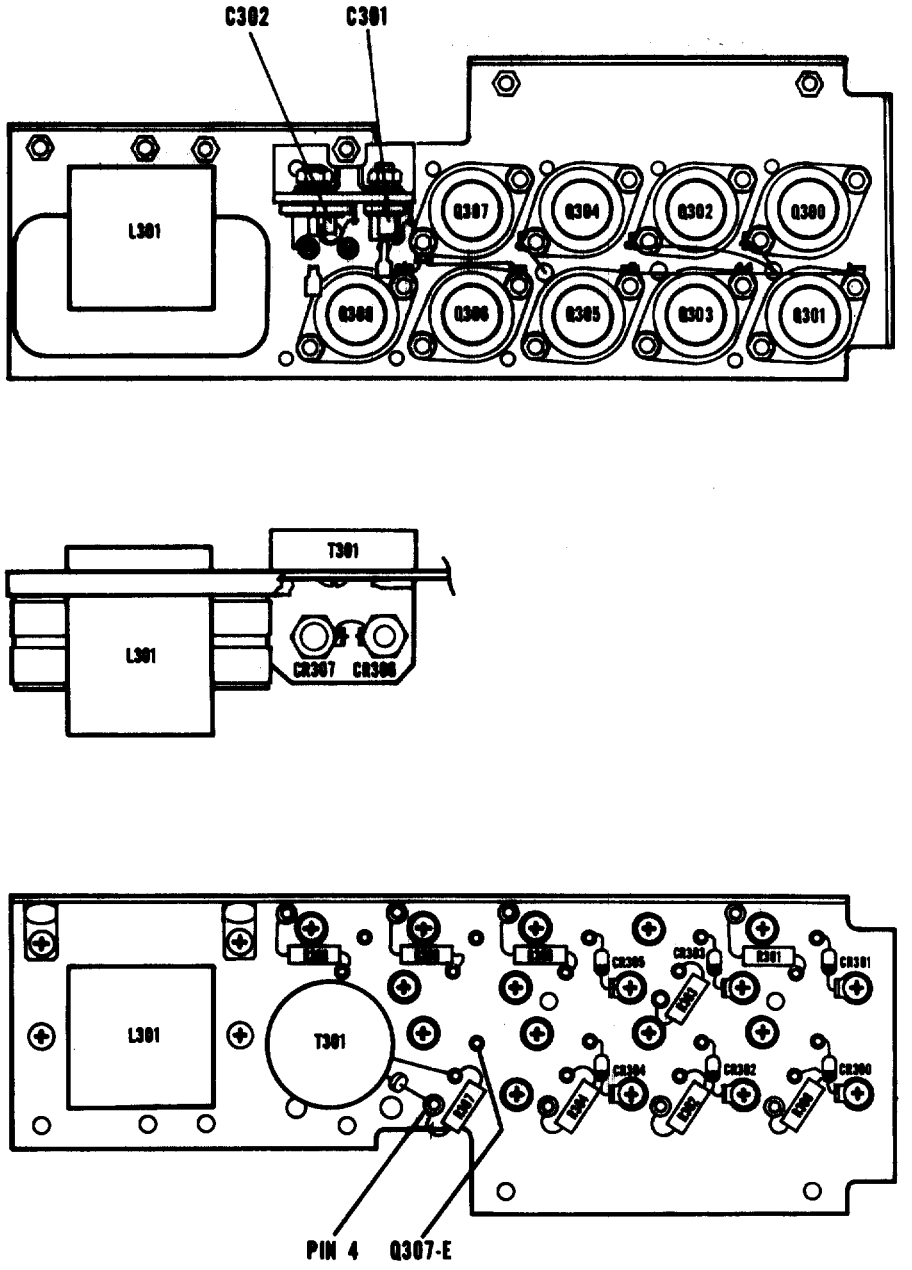


Figure 3-11. High Level Boost Module A2.



EL7PI021

Figure 3-12. Low Level Boost Module A3.

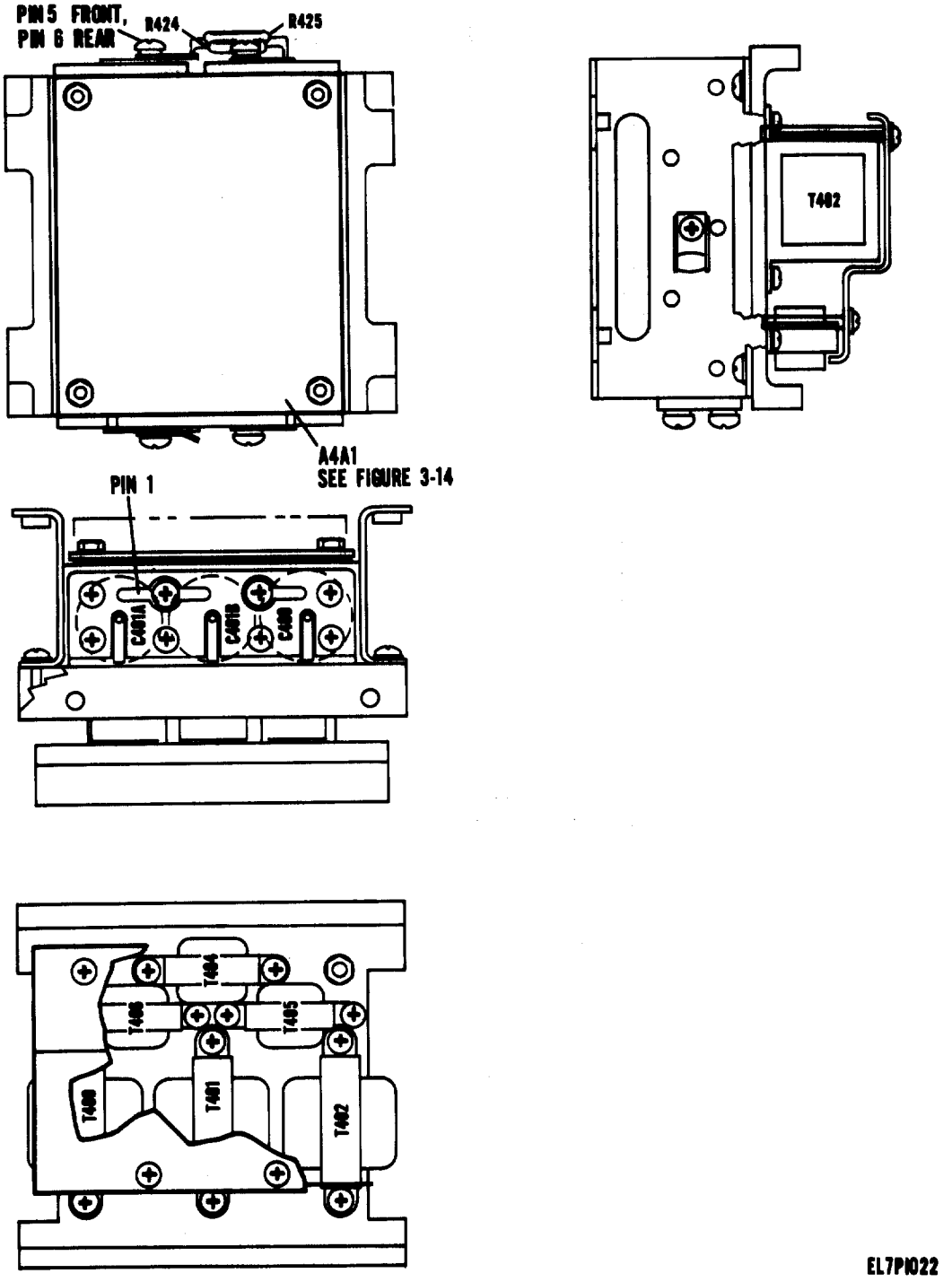


Figure 3-13. Power Capacitors and Driver Module A4.

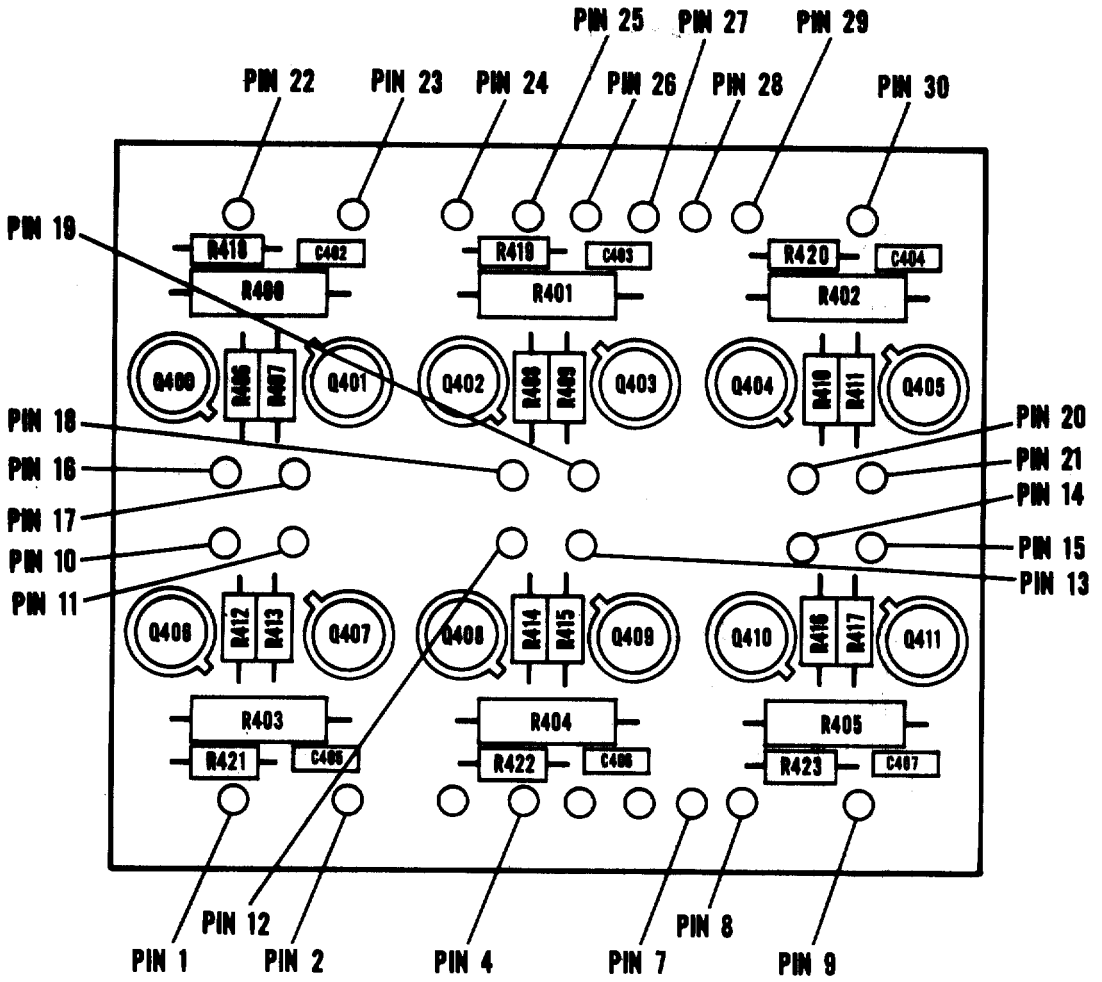
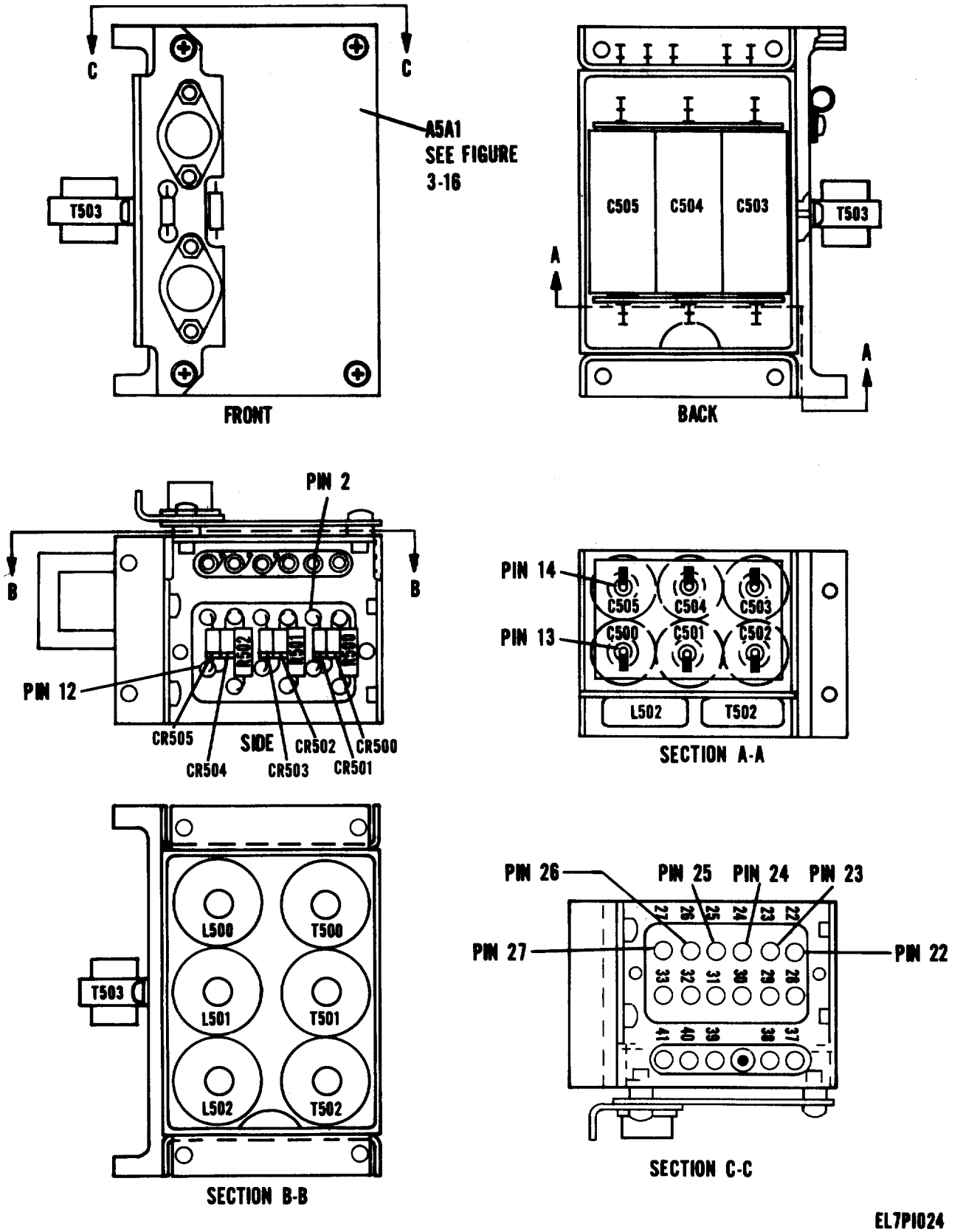


Figure 3-14. Component Assembly A4A1.



Regular 3-l5. Output Filters and Bias Regulator Module A5.

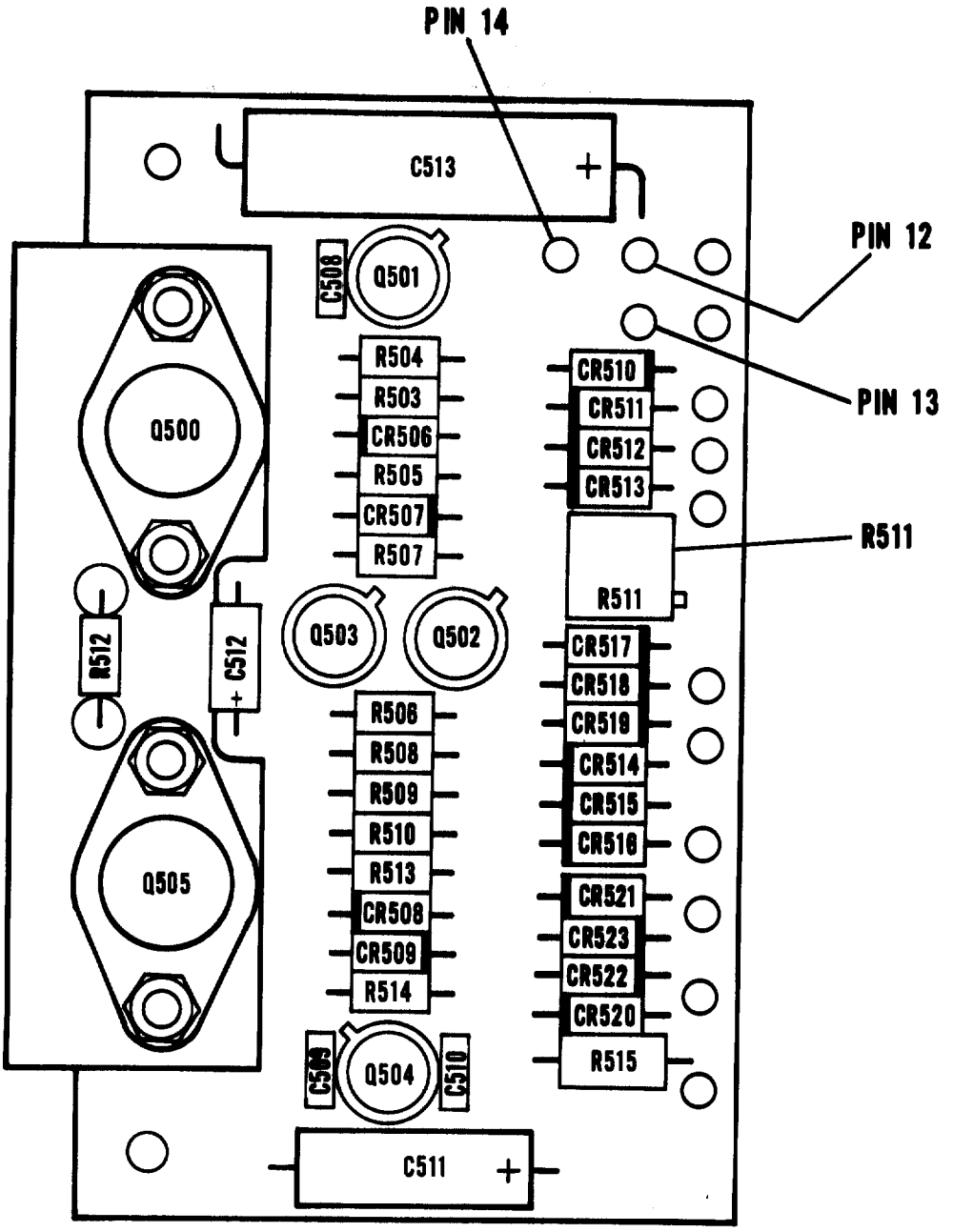


Figure 3-16. Component Assembly A5A1.

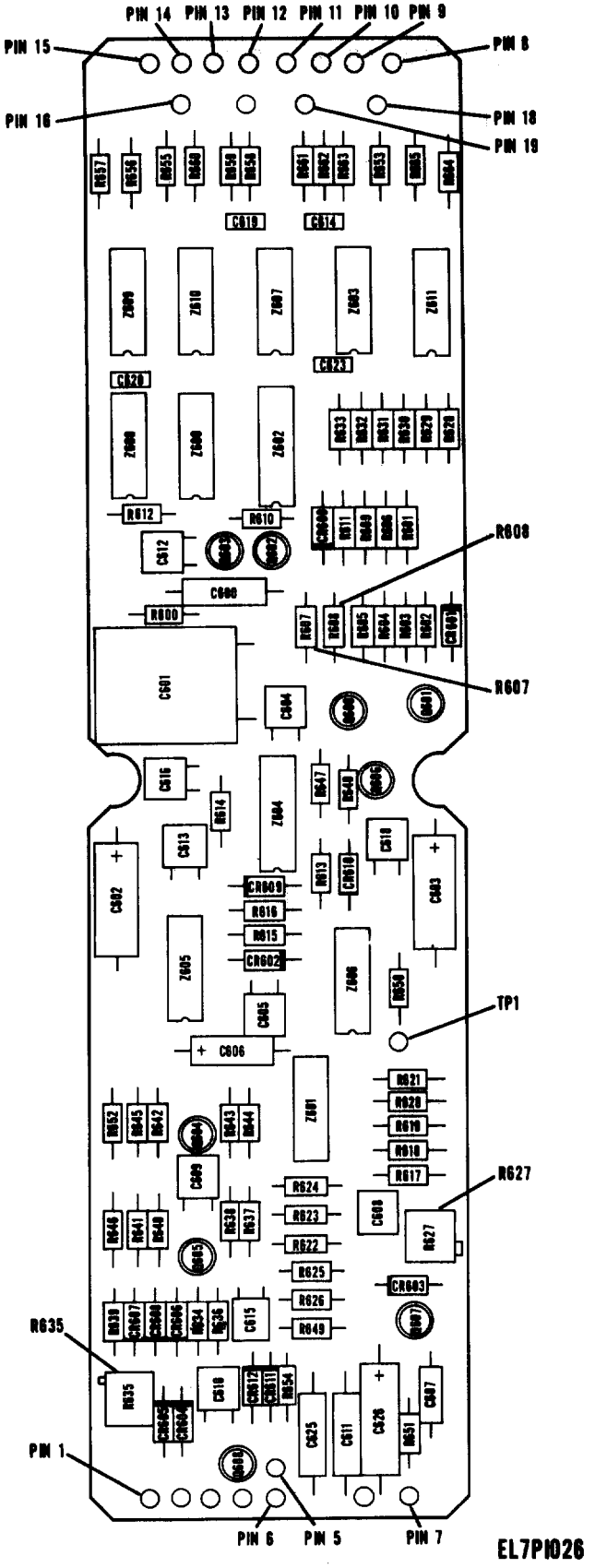


Figure 3-17. Logic Component Assembly A6.

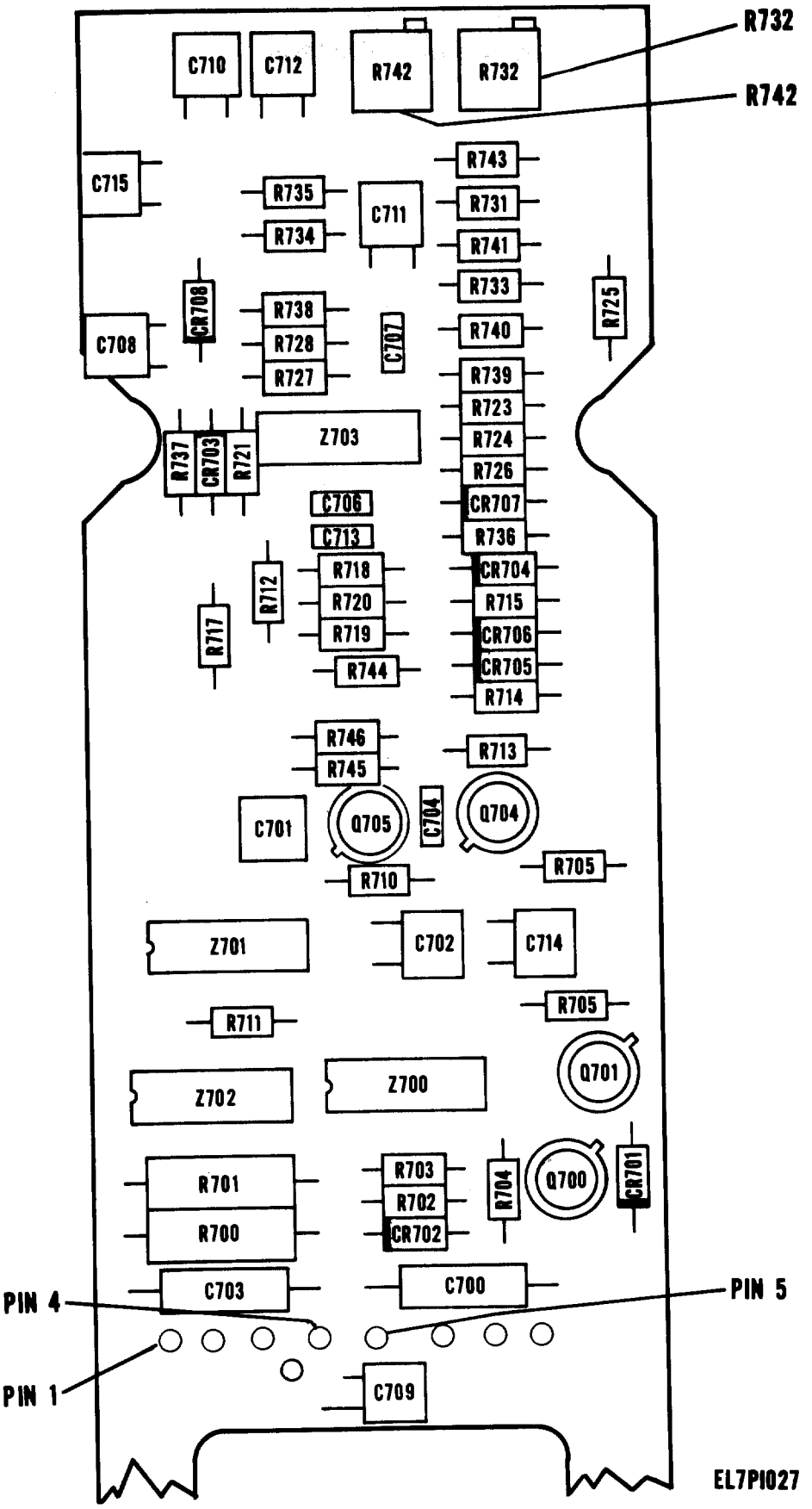


Figure 3-18. Boost Regulator Component Assembly A7.

3-5. Test Setup

connect fully assembled and closed inverter to test fixture as shown in figure 3-19 (refer to fig. FO 3-20 for test fixture schematic).

3-6. Procedure

Perform the following instructions to determine that the inverter meets operational parameters. There are no inverter adjustments and alignments nor calibration that should be performed during this operational checkout. The initial switch positions of the test fixture shall be as indicated on figure 3-19 prior to performing the instructions below.

a. Set the DELTA/1ØWYE switch S21 to DELTA position.

b. Set the UNIT PWR switch S6 to ON position and apply 18 vdc input from the input power supply.

c. Set OUTPUT MONITOR switch S16 to A position.

d. Read the output phase voltage indicated on Digital Voltmeter AN/USM-281 No. 4. The output voltage shall be between 100 and 117.5 vrms.

NOTE

The test setup and text specified the use of four digital voltmeters for simplicity. Only one digital voltmeter need be used and connected, in turn, to any of the four monitoring terminals on the test fixture.

e. Read the percent distortion of output phase as indicated on Distortion Analyzer TS-723/A. The distortion shall be **5** percent maximum.

f. Read the output phase frequency as indicated on Electronic Counter AN/USM-207. The frequency shall be between 393 and 407 Hz.

g. Set OUTPUT MONITOR switch S16 to B and C positions respectively and at each position repeat , *d* through *f* above for the ØB and ØC outputs.

h. Increase the input power supply voltage to 26 vdc and 29 vdc respectively, and for each input voltage repeat *c* through *g* above.

i. Set UNIT PWR switch S6 to OFF position.

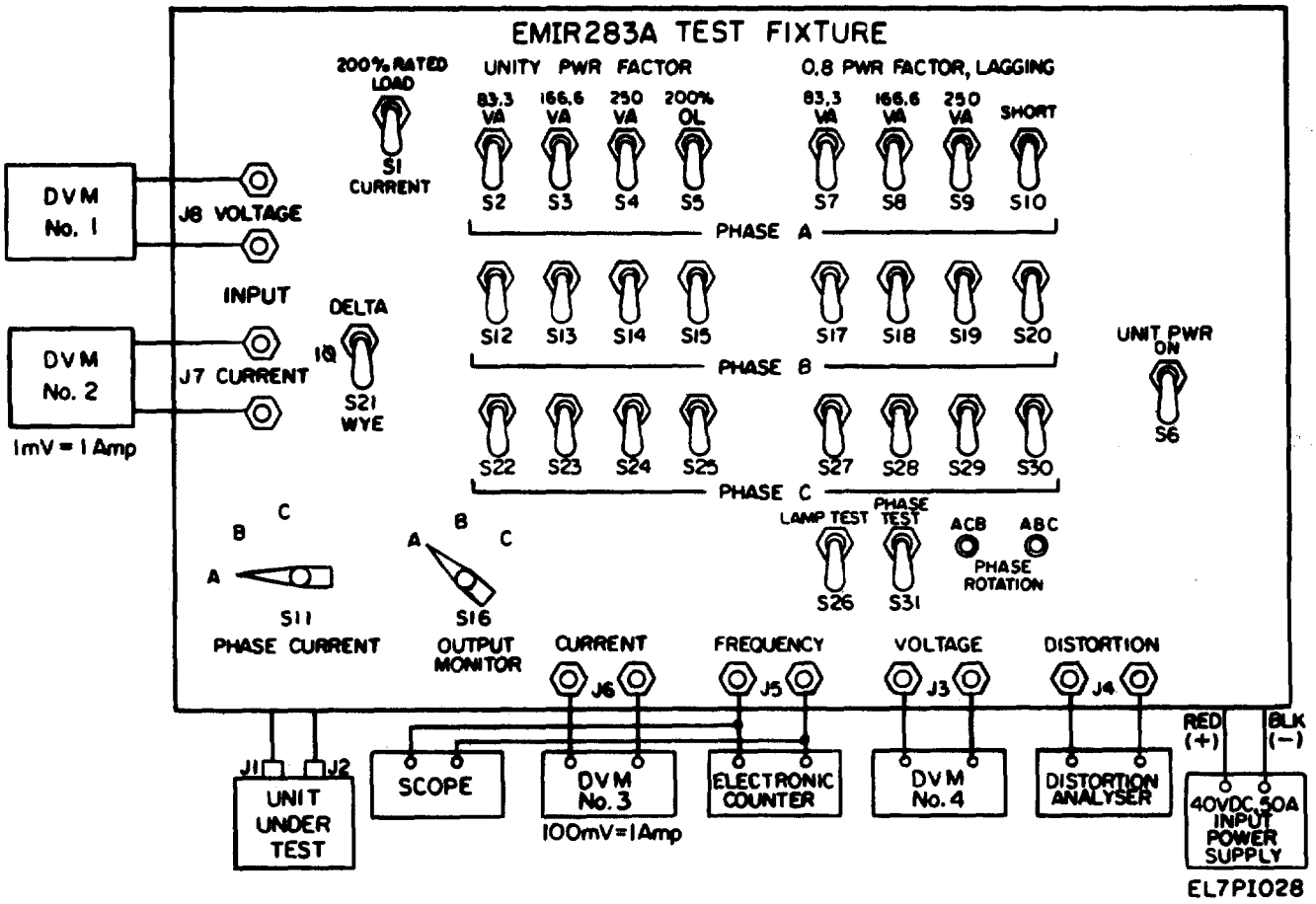


Figure 3-19. Final Test Setup.

j. Set switches S2, 3, 4, 12, 13, 14, 22, 23 and 24 to the up (on) position (250 VA, Unity P.F. Loads) and repeat b through *i* above.

k. Set switches S2, 3, 4, 12, 13, 14, 22, 23 and 24 to the down (off) position and switches S7, 8, 9, 17, 18, 19, 27, 28 and 29 to the up (on) position (260 VA, .8 P.F. Lagging Loads) and repeat *b* through *i* above.

l. Set switch S2 to the Up (on) position, switches S7, 8, 9, 17, 18, 19, 27, 28 and 29 to the down (off) position, and DELTA/1Ø/WYE switch S21 to WYE position.

m. Set UNIT PWR switch S6 to ON position and apply 26 vdc input from the power supply.

n. Set OUTPUT MONITOR switch S16 to A, B and C positions respectively and at each position read the corresponding phase output voltage indicated on digital Voltmeter No. 4. The ØA, ØB and ØC output voltages shall be between 110 and 120 vrms.

o. Increase the input power supply voltage to 29 vdc and repeat *n* above. Set UNIT PWR switch S6 to OFF position.

p. Set switches S3, 4, 12, 13, 22, 23 and 24 to the up(on) position (Unbalanced, Unity P.F. Loads. Repeat *m*, *n* and *o* above.

q. Set switches S2, 3, 4, 12, 13, 14, 22, 23 and 24 to the up(on) position (250VA, Unity P.F. Load). 1

r. Set DELTA/1Ø/WYE switch S21 to DELTA position.

s. Set UNIT PWR switch S6 to ON position and apply 28 vdc input from the input power supply.

t. Set LAMP TEST switch S31 to LAMP TEST position.

u. Set TEST switch S26 to TEST position. The ACB and ABC, PHASE ROTATION indicators shall illuminate.

v. With TEST switch S26 in TEST position, set LAMP TEST switch S31 to down position. The ACB PHASE ROTATION indicator shall extinguish and the ABC indicator shall illuminate.

w. Adjust input voltage between 27.5 and 28.5 vdc as indicated on digital voltmeter No. 1. Note actual input voltage.

x. Using the digital voltmeter red the input current equivalent millivolts (1 mV = 1 amp) as indicated on digital voltmeter No. 2 Record input current.

y. Calculate input power in watts ($P_{IN} = V_{IN} X I_{IN}$) and record result.

z. Set OUTPUT MONITOR switch S16 to A, B and C positions respectively and at each position read the corresponding phase output voltage (ØA V_{OUT}, ØB, V_{OUT} and ØC V_{OUT}) on digital voltmeter No. 4. Record output voltages.

aa. Set UNIT PWR switch S6 to OFF position.

ab. Calculate the power-out in watts using the following formula:

$$\frac{ØA\ V^2_{OUT}}{53.81} + \frac{ØB\ V^2_{OUT}}{53.81} + \frac{ØC\ V^2_{OUT}}{53.81} = P_{OUT}$$

ac. Calculate the pencent inverter efficiency using the following formula:

$$\%\ \text{Efficiency} = \frac{P_{OUT}(\text{step bb})}{P_{IN}(\text{step Y})} \times 100$$

The inverter efficiency shall be 65 percent minimum.

ad. Set PHASE CURRENT switch S11 and OUTPUT MONITOR switch S16 to A position.

ae. Set 200% OL switches S5, 15 and 25 to the up(on) position.

af. Set UNIT PWR switch S6 to ON position and apply 26 vdc input from the input power supply.

ag. Set 200% RATED LOAD CURRENT switch S1 to the up(on) position.

ah. Before ØA output current foldback (digital voltmeter No. 3 reads 100 mV or less), measure the following ØA parameters. (The output current foldback occurs in 5 to 15 seconds after switch S1 is set to 200% RATED LOAD position. If necessary, reset output overload condition to enable measurement of listed parameters.)

(1) Read output voltage as indicated on digital voltmeter No. 4. The output voltage shall be 60 vrms or less.

(2) Read the output current equivalent millivolts (100 mV = 1 amp) as indicated on digital voltmeter No. 3. The output current shall be 4.34 amps or greater.

(3) Read the output frequency as indicated on electronic counter. The output frequency shall be between 393 and 407 Hz.

ai. Set 200% RATED LOAD CURRENT switch S1 to the down (off) position.

aj. Set PHASE CURRENT switch S11 and OUTPUT MONITOR switch S16 to B position.

ak. Before ØB output current foldback (digital voltmeter No. 3 reads 100 mV or less), measure the following ØB parameters. (The output current foldback occurs in 5 to 15 seconds after witch S1 is set to 200% RATED LOAD position. If necessary, reset output overload condition to enable measurement of listed parameters.)

(1) Read output voltage as indicated on digital voltmeter No. 4. The output voltage shall be 50 vrms or less.

(2) Read the output current equivalent millivolts (100 mV = 1 amp) as indicated on digital voltmeter No. 3. The output current shall be 4.34 amps or greater,

(3) Read the output frequency as indicated on electronic counter. The output frequency shall be

between 393 and 407 Hz.

al. Set 200% RATED LOAD CURRENT switch S1 to the down (off) position.

am. set PHASE CURRENT switch S11 and OUTPUT MONITOR switch S16 to C position.

an. Bfore ØC output foldback (digital voltmeter No. 3 reads 100 mV or less), measure the following ØC parameters. (The output current foldback occurs in 5 to 15 seconds after switch S1 is set to 200% RATED LOAD position. If necessary, reset output overload condition to enable measurement of listed parameters.)

(1) Read Output voltage as indicated on digital voltmeter No. 4 The output voltage shall be 50 vrms or less.

(2) Read the output current equivalent millivolts (100 mV = 1 amp) as indicated on digital voltmeter No. 3. The output current shall be 4.34 amps or greater.

(3) Read the output frequency as indicated on electronic counter. The output frequecy shall be between 393 and 407 Hz.

ao. Set 200% RATED LOAD CURRENT switch S1 to the down (off) position and set UNIT PWR switch S6 to OFF position.

ap. Set switches S2, 3, 4, 12, 14, 22, 23 and 24 to the down (off) position.

aq. Set switches S7, 8, 9, 17, 18, 19, 27, 28 and 29 to the up (on) position (250 VA, 0.75 P.F. Load).

ar. Set UNIT PWR switch S6 to ON position and apply 26 vdc input from the input power supply.

as. Set the OUTPUT MONITOR swith S16 to A position and SHORT swith S10 to the up(on) position.

at. Before ØA output currant foldback (digital voltmeter No. 3 reads 100 mV or less), read the output current equivalent millivolts (100 mV = 1 amp) as indicated on digital voltmeter No. 3. The output current shall be 5.43 amps or greater.

au. set the OUTPUT MONITOR switch S16 to B Position, SHORT switch S10 to the down (off) position and S20 to the up (on) position.

av. Before ØB output current foldback (digital voltmeter No. 3 reads 100 mV or less), read the output current equivalent millivolts , (100 mV = 1 amp) as indicated on digital voltmeter No. 3. The output current shall be 5.43 amps or greater.

aw. Set the OUTPUT MONITOR switch S16 to C position, SHORT switch S20 to the down (off) position and S30 to the up(on) position.

ax. Before ØC output current foldback (digital voltmeter No. 3 ready 100 mV or less), read the output current equivalent millivolts (100 mV = 1 amp) as indicated on digital voltmeter No. 3 The output current shall be 5.43 amp or greater.

ay. Set UNIT PWR switch S6 to OFF position, deenergize input power supply and remove unit from test setup.

Section II. TOOLS AND EQUIPMENT

3-7. Tools and Equipment

The following instruments or equivalent are required to perform the inverter operational checkout:

a. Dc power supply, any commercial type providing 0 to 45 vdc, 6 amps maximum.

b. DC Power supply, any commercial type providing 0 to 40 vdc, 50 amps maximum.

c. Oscilloscope AN/USM-281

d. Digital Voltmeter AN/GSM-64

e. Electronic Counter AN/USM-207

f. Distortion Analyzer TS-723/A

g. EM1289A Test Fixture, Gulton No. 421773

Section III. TROUBLESHOOTING

3-8. Troubleshooting

Use table 3-2 to troubleshoot the inverter to the module level or to the component part level. Then replace either entire defective module or defective component part. Note that initial digit of the part number is also the module number. For example, transistor Q206 is a component of the A2 module. Refer to paragraphs 3-9 and 3-10 for information on complete disassembly/assembly of inverter.

Table-3-2. Troubleshooting Data

MALFUNCTION	PROBABLE CAUSE	CORRECTIVE ACTION
Inverter input terminals pins A and C of J1 shorted	Transistor Q206, Q207, Q208, Q306, Q307, Q308, Q200 through Q205 and Q300 through Q305; diode CR200 through CR205 and CR3OO through CR305 shorted.	Replace defective component, or defective A2 (A3 module)
Inverter will not turn on (no output voltage).	Transistor Q500 through Q505, Q605; diode CR510 through CR519, integrated circuit Z608 defective.	Replace defective component, or defective A5/A6 module,
Inverter draws excessive input current.	Capacitor C400, C401A and/or C401B defective,	Replace defective A4 module.
No output voltage regulation at no-load.	Diode CR206, CR207, CR306 and CR307 open; Transistor Q206, Q207, Q208, Q306, Q307, Q308, Q700 and Q701 open; integrated circuit Z700, Z702 and Z703 defective.	Replace defective component, or defective A2/A3/A7 modules.
Poor output voltage regulation at full load.	Check set-in test calibration for potentiometers R732 and R742; diodes CR520 through CR523; integrated circuit Z703 defective.	Replace defective component, or defective A7/A5 module.
Output frequency drifts with input voltage change.	Transistor Q600, Q601, Q602 and Q603; diode CR600 and CR601 defective.	Replace defective component, or defective A6 module.
Output frequency out-of-tolerance.	Check set-in-test calibration for resistors R607 and R608; integrated circuit Z600 defective.	Replace defective component, or defective A6 module.
High distortion for any one of the three phases.	Capacitor C500 and C505, or C501 and C504 or C502 and C503; Choke L500, L501 and L502 defective.	Replace defective A5 module.
High distortion for all three phases.	Transistor Q200 through Q205, Q300 through Q305, Q400 through Q411; integrated circuit Z603, Z607 through Z611 defective.	RepIace defective component, or defective A2/A3/A4/A6 module.
Low efficiency.	Transistor Q200 through Q205, Q300 through Q305, Q400 through Q411 defective.	Replace defective component, or defective A2/A3/A4 module.
Insufficient overload capacity.	Diodes CR200 through CR205, CR300 through CR305 defective.	Replace defective component, or defective A2/A3 module.

3-9. (Complete Disassembly of Inverter

Perform only as much of this procedure as necessary to remove or test the suspected defective assembly or component. Be sure no power is applied to inverter during disassembly.

NOTE

Use normal shop practice of unsoldering (or unscrewing wire terminal) and tagging (identifying) all interconnecting wires that must be detached to disassemble inverter. During assembly the tagged information will enable wires to be soldered back in place or the wire terminal to be screwed back into proper location.

a. Remove bottom cover (14, fig. 3-21) by removing six screws (19).

b. Remove top cover (1) by removing 34 screws (3) and 34 flat washers (2).

c. Remove rear cover (9) by removing three screws (3) and three washers (2); and removing four screws (3), four lockwashers (7) and four flat washers (2).

d. Remove Al module (33) by removing three screws (3) and three flat washers (2); and removing four screws (32), four lockwashers (7) and four flat washers (2).

e. Remove A5 module (34) by removing two screws (32), two lockwashers (7) and two flat washers (2); and removing two screws (8), two lockwashers (7), two flat washers (2) and two cable clamps (4 and 6).

f. Remove A4 module (5) by removing four screws (8), four lockwashers (7), four flat washers (2) and four cable clamps (4 and 6).

g. Remove A3 module (27) by removing five screws (3) and five flat washers (2).

NOTE

In order to remove the two screws (3) on front (fan) side of A2 module it will be necessary to temporarily remove two screws, two lockwashers, two flat washers and two cable clamps on A2 module which block access to the two front screws (3). Replace these items after the two front screws (3) are removed.

h. Remove A2 module (26) by removing five screws (3) and five flat washers (2).

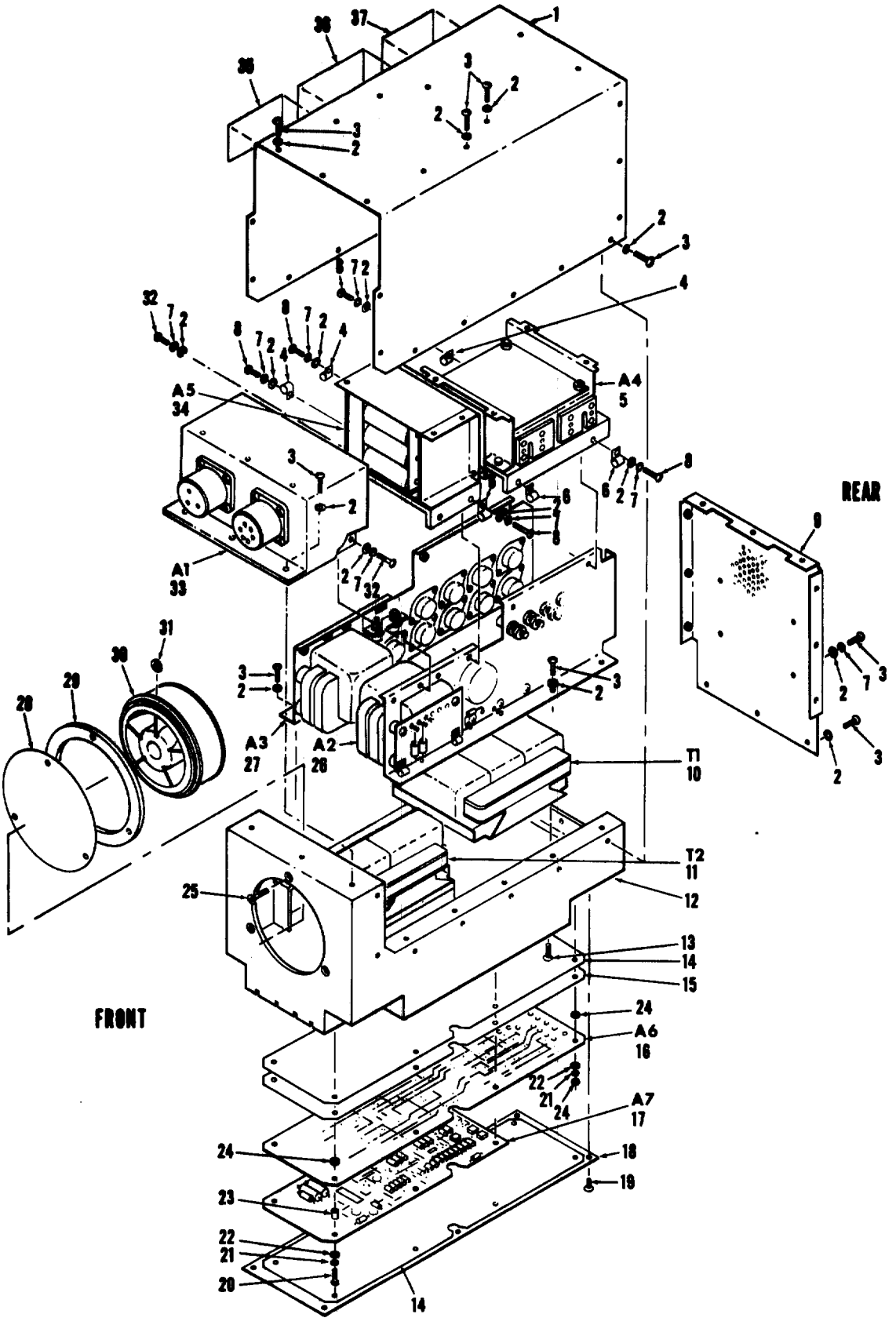


Figure 3-21. Static Inverter Complete Disassembly/Assembly.

i. Remove fan assembly by removing three screws (25), three synclamps (31), front screen (28), fan adapter (29) and fan (30).

j. Remove A7 component assembly (17) by removing six screws (20), six lockwashers (21) and six flat washers (22).

NOTE

Hardware removed in *k* and *l* below is associated with housing (12) studs.

k. Remove A6 component assembly (16) by removing six spacers (23), two nuts (24), two lockwashers (21), and two flat washers (22).

l. Remove unclad board (15) and clad board (14) by removing eight nuts (24).

m. Remove transformer T1 (10) by removing four screws (13).

n. Remove transformer T2 (11) by removing four Screws (13).

o. All modules, component assemblies and parts are now disassembled from housing (12).

3-10. Complete Assembly of Inverter

NOTE

Position large transformer T1 (10), fig. 3-21) so leads 1 through 3 are on same side of housing (12) as A2 model (26).

a. Install transformer T1(10) on housing (12) with four screws (13).

NOTE

Position small transformer T2(11) so leads 4 through 15 are on same side of housing (12) as A2 assembly (26).

b. Install transformer T2 (11) on housing (12) with four screws (13).

NOTE

Hardware installed in *c* and *d* below is installed on housing (12) studs.

c. Install unclad board (15) and clad board (14) on housing (12) with eight nuts (24).

d. Install A6 component assembly (16) on housing (12) with six spacers (2), two nuts (24), two lockwashers (2) and two flat washers (22).

e. Install A7 component assembly (17) on housing (12) with six screws (20), six lockwashers (21) and six flat washers (22).

f. Install fan assembly on housing (12), as follows: line up front screen (28), fan adapter (29) and fan (30) on inside of housing (12); install parts with three screws (25) and three synclamps (31).

NOTE

In order to install the two screws (3) on front (fan) side of A2 module it will be necessary to temporarily remove two screws, two lockwashers two flat washers and two cable clamps on A2 module which block access to the two front screws (3). Replace these items after the two front screws (3) are installed.

g. Install A2 module (26) on housing (12) with five screws (3) and five flat washers (2).

h. Install A3 mosulw on housing (12) with five screws (3) and five flat washers (2).

i. Install A4 module (5) with four screws (8), four lockwashers (7), four flat washers (2) and four cable clamps (4 and 6).

j. Install A5 module (34) with two screws (32), two lockwashers (7) and two flat washers (2); and two screws (8), two lockwashers (7), two flat washers (2) and two cable clamps (4 and 6).

k. Install Al module with three screws (3) and three flat washers (2); and four screws (32), four lockwashers (7) and four flat washers (2).

l. Install rear cover (9) with three screws (3) and three washers (2); and four screws (3), four lockwashers (7) and four flat washers (2).

m. Install bottom cover (18) with six screws (19)

n. Install top cover (1) with 34 screws (3) and 34 flat washers (2).

Section IV. MAINTENANCE

WARNING

High voltages and currents are present on disassembled inverter when it is energized. Do not touch any exposed wiring or any metal point inside inverter. Lethal shock could result.

3-11. General

Adjusts listed in paragraphs 3-12 through 3-15 may be performed individually, as needed, or may be performed in the sequence given.

3-12. Bias Regulator Voltage Adjustment (R511)

a. Remove top cover (1, fig. 3-21) by removing 34 screws (3) and 34 flat washers (2).

b. Unsolder wire at pin (13) of component assembly A5Al (see fig.3-16).

c. Connect a 30 vdc, 0-5 amps power supply to pins 13(+) and 14(-) of component assembly A5A1.

d. connect Digital voltmeter AN/GSM-64 to pins 12(+) and 14-) of component assembly A5A1.

e. Adjust power supply voltage to 25.0 ±1.0 vdc. Adjust potentiometer R511 until the digital voltmeter indicates 14.00 ±0.01 vdc.

f. Disconnect 30 vdc power supply and digital voltmeter. Resolder wire to pin 13 of component assembly A5A1.

g. Install top cover (1, fig. 3-21) with 34 screws (3) and 34 flat washers (2).

3-13. Front Loop and Back Loop Adjustment (R732 and R742)

a. Remove bottom cover (18, fig. 3-21) by removing six screws (19).

b. Connect inverter to test fixture in accordance with fig. 3-19.

c. On component assembly A7 (fig. 3-18) adjust potentiometer R732 (front loop adjustment) and potentiometer R742 (back loop adjustment) full Counterclockwise.

d. On test fixture, set UNIT PWR switch S6 to ON position and gradually apply +28.0 ±2.0 vdc.

e. Adjust potentiometer R732 clockwise until Digital Voltmeter AN/GSM-64 No. 4 indicates 115.0 ±0.1 vdc.

f. Set switches S2, 3, 4, 12, 13, 14, 22, 23, 24 to the up (on) position to apply 250 VA load on all three output phases. Adjust potentiometer R742 until digital voltmeter No. 4 indicates 115.0 ±9.1 vdc.

g. Set switches S2, 3, 4, 12, 13, 14, 22, 23, 24 to the down (off) position (no load). Adjust potentiometer R732 until digital voltmeter No. 4 reads 115.0 ±0.1 vdc.

h. Repeat *d* through *g* above until the output voltage regulation from no load to 250 VA is within 0.1 vac.

i. Deenergize the input power supply and disconnect inverter from test fixture.

j. Install six screws (19, fig. 3-21) and bottom cover (18).

3-14. Frequency and Protective Circuit Reference Voltage Adjustment (R627)

a. Remove bottom cover (18, fig. 3-21) by removing Six screws (19).

b. Loosen A7 component assembly (17) by removing six screws (20), six lockwashers (21) and six flat washers (22).

c. Place unit with front side down on workbench.

CAUTION

When performing *d* and *e* below, make sure components, pin and printed wiring on A7 component assembly (17) do not touch chassis ground; do not damage interconnecting wiring.

d. Carefully lay back upper end of A7 assembly (17) 90 degrees over on to work bench; do not put strain on interconnecting wiring.

e. Loosen A6 component assembly (16) by removing six spacers (23); and two nuts (24), two lockwashers (21) and two flat washers (22).

f. Carefully move lower end of A6 component assembly (16) a few inches forward as necessary to gain access to adjustment screws of R627 (and R635 for para 3-15) potentiometers (see fig. 3-17); do not put strain on upper interconnecting wiring.

g. Connect Digital Voltmeter AN/GSM-64 to pins TP1(+) (fig. 3-17) and 7 (-) of component assembly A6.

h. Connect Oscilloscope AN/USM-281 and Electronic Counter AN/USM-207 to pins 15 (+) and 12(–).

i. Connect inverter to test fixture in accordance with fig. 3-19.

j. Set UNIT PWR switch S6 to ON position and apply 25 ±1 vdc to input as read on digital voltmeter No. 1.

k. Adjust potentiometer R627 for an indication of 4.000 ±0.005 on the digital voltmeter.

l. The oscilloscope shall display a waveform as shown in figure 3-2 and the electronic counter shall indicate 400 ±1 Hz.

m. If the electronic counter does not read 400 ±1 Hz, change resistor R608 value to obtain a frequency indication of 400 ±1 Hz.

n. Set UNIT PWR switch S6 to down (off) position and disconnect digital voltmeter, oscilloscope and electronic counter.

o. Disconnect inverter from test fixture.

NOTE

Perform *p*, *q*, and *r* below only if paragraph 3-15, input overvoltage adjustment, will not be performed next. If it will be performed, go directly to paragraph 3-15.

p. Install A6 component assembly (16, fig. 3-21) to housing (12) studs with six acers (23); and two nuts (24), two lockwashers (21) and two flat washers (22).

q. Carefully lay A7 component assembly (17) back in place on top of A6 assembly (16); be careful of interconneting wiring. Install A7 component

assembly with six screws (20), six lockwashers (21) and six flat washers (22).

r. Install bottom cover (18) on housing (12 with six screws (19).

3-15. Input Overvoltage Adjustment (R635)

a. If not already performed, perform disassembly procedures in paragraph 3-14 *a* through *f*.

b. Connect Oscilloscope AN/USM-281 to pins 15(+) and 7(-) of component assembly A6 (fig. 3-17).

c. Turn potentiometer R635 fully counterclockwise.

d. connect inverter to test fixture per figures 3-19.

e. Set UNIT PWR switch S6 to ON position and adjust input to 44 ±0.5 vdc as read on digital voltmeter AN/GSM-64 No. 1.

f. Slowly adjust potentiometer R635 clockwise until the oscilloscope waveform goes to 0 volts.

g. Set UNIT PWR switch to S6 to down (off) position.

h. Disconnect oscilloscope from inverter.

i. Perform assembly procedures in para 3-14 *p*, *q*, and *r*.

3-16. Repair Materials

Paragraphs 8-17 through 3-19 contain procedures for using repair materials which are needed when replacing certain component parts. Table 3-3 lists the repair materials; table 3-4 lists the component parts and their location; pargraphs3-17 through 3-19 contain instructions for preparing and using the repair materials.

Table 3-3. Repair Materials

MATERIAL	TYPE	SOURCE
Paint	Flat Black	Commercially available
Solder	SN60-40	Kester Solder Company 4201 Wrightwood Ave. Chicago, IL FSCM 75295
Adhesive, Staking	Epocast 202	Furane Plastics, Inc. 5121 San Fernando Rd. Los Angeles, CA 90039 FSCM 99384
Brush	Artist, small	Commercially available
Tuluol/Toluene	Anhydrous Reagent Grade	VanWaters and Rogers 1363 S. Bonnie Beach Pl. Los Angeles, CA FSCM 08455
Conformal Coating	1B31, Humiseal	Columbia Chase Corp. Humiseal Division Woodside, New York 11377
Isopropyl Alcohol	MIL-I-10428	Commercially available
Silicone Rubber	RTV-615 A & B	General Electric Silicone Products Dept. Waterford, NY 12188 FSCM 01139
Diluent	RTV-910	
Microballoon Sphere	1G-101	Emerson & Cumings Canton, MA 02021 FSCM 04552

Table3-4 Cross Reference To Module/Component assemblies Needing Repair Materials

MODULE/COMPONENT ASSEMBLY	REPAIR PROCEDURE AND COMPONENT PARTS
EMI MODULE Al (fig. 3-10)	Capacitors C100 through C104 and C106 through C109 are secured with a fillet of Epocast 202 (100 parts of 202).
HIGH LEVEL BOOST MODULE A2 (fig. 3-11)	*a*. Capacitors C201 and C202 are secured with a fillet of Epocast 202 (100 parts of 202). *b*. A2 module is conformal coated with 1B31 (Humiseal), both sides.
LOW LEVEL BOOST MODULE A3 (fig. 3-12	*a*. Capacitors C301 and C302 are secured with a fillet of Epocast 202 (100 parts of 202). *b*. A3 module is conformal coated with 1B31 (Humiseal), both sides.

Table 3-4 Cross Reference To Module/Component Assemblies Needing Repair Materials-Continued

MODULE/COMPONENT ASSEMBLY	REPA1R PROCEDURE AND COMPONENT PARTS
POWER CAPACITORS AND DRIVER MODULE A4 (fig. 3-13)	*a.* Resistors R424 and R425 are secured with a fillet of Epocast 202 (101 parts of 202). *b.* Plate SP04B-112B24 is secured across transformer T402 core with Eocast 202 (100 parts of 202).
COMPONENT ASSEMBLY A4A1 (fig. 3-14)	*a.* Transistors, Q400 through Q411 are secured with Epocast 202 (100 parts of 202). *b.* A4A1 is conformal coated with 1B31 (Humiseal), both sides.
COMPONENT ASSEMBLY A4A1 (fig. 3-16)	*a.* Capacitors C51l and C513 are secured with a fillet of Epocast 202 (100 parts of 202). *b.* A5A1 is conformal coated with 1B31 (Humiseal).
LOGIC COMPONENT ASSEMBLY A6 (fig. 3-17)	A6 component assembly is conformal coated with 1B31 (Humiseal), both sides.
BOOST REGULATOR COMPONENT ASSEMBLY A7 –	A7 component assembly is conformal coated with 1B31 (Humiseal), both sides.

3-17. Nonformal Coating with 1B31 (Humiseal)

The following procedure shall apply to the replacement of a comformal coated component mounted on either a module or component assembly.

WARNING

Do not use 1B31 and Tuluol/Toluene in presence of open flame or sparks. Avoid inhalation of vapors. Adequate ventilation to the outdoors is necessary. Prevent contact with eyes and skin. If contact occurs, wash with soap and water.

a. Dissolve existing 1B31 from small rework area with isopropyl alcohol and cotton swab stick.

b. Replace the defective part using good workmanship standards.

c. Replace the conformal coating with Type 1B31 used full strength from its container. Shelf life of 1B31 in the container is six months at room temperature. 1B31 maybe thinned with Tuluol/Toluene to adjust thickness, if necessary. Expose only quantities of 1B31 to the atmosphere that will be used within 1-1/2 hours. Any material that has been exposed 1-1/2 hours, or more, shall be scrapped. Material shall be stored at room temperature, away from excessive heat.

d. Apply a thin coat of conformal coating to the affected area, overlapping the existing coat about 1/16 of an inch to obtain a moisture seal. A short artist brush will serve as an applicator.

e. Allow ten minutes air drying before handling. Apply heat by means of an infra-red heat lamp, forced-air heat gun or cure in oven. Object is to increase the surface temperature of the coated area to 170°F ±5°F for one hour.

f. After the application and cure of conformal coating, inspect repair area for any blistering, wrinkling, cracking or peeling of coating. If any of the above is evident, perform repair procedure again.

g. After all areas are repaired, the board can be reinstalled in its permanent position.

3-18. Use of Epocast 202

To accomplish repair of the components which are held with Epocast 202, proceed as follows.

NOTE

Required mix of either 100 parts or 60 parts of resin 202 is specified in table 3-4.

a. Preparation of Epocast 202. Combine 100 parts by weight of hardener 9615 with 60 or 100 parts by weight of resin 202 and stir thoroughly until a uniform color is obtained. Mix only quantities which will be used within 2-1/2 hours. If not used within 2-1/2 hours, discard mixed material.

b. Repair Using Epocast 202.

CAUTION

Use care in heating Epocast 202 not to damage nearby components. Use either 50 watt max soldering iron or heat gun, whatever will cause the least heating of components.

(1) Heat area of Epocast 202 with 50 watt max soldering iron or heat gun until material is soft. Lift small component away from material. While still soft, remove material using a non-metallic tool. Clean area of grease, oil, flux and contamination with soft brush and isopropyl alcohol.

(2) When a fillet bond is required, apply fillet along the length of component. A thin layer of adhesive may blend over a portion of the body of the component. When components must be encapsulated, apply adhesive (5 to 20 mils thick) over the entire mounting surface of the components.

(3) Cure adhesive for two to four hours at 150 ±10°F or for 24 hours at room temperature. Clamp

component to mounting surface to maintain contact presure throughout the cure time.

(4) After the cure of adhesive, inspect repair area for any cracks, voids, bubbles or other defects. If any of the above is evident, perform repair procedure again,

Section V. DIRECI' SUPPORT TEST PROCEDURES

2-19. Final Test

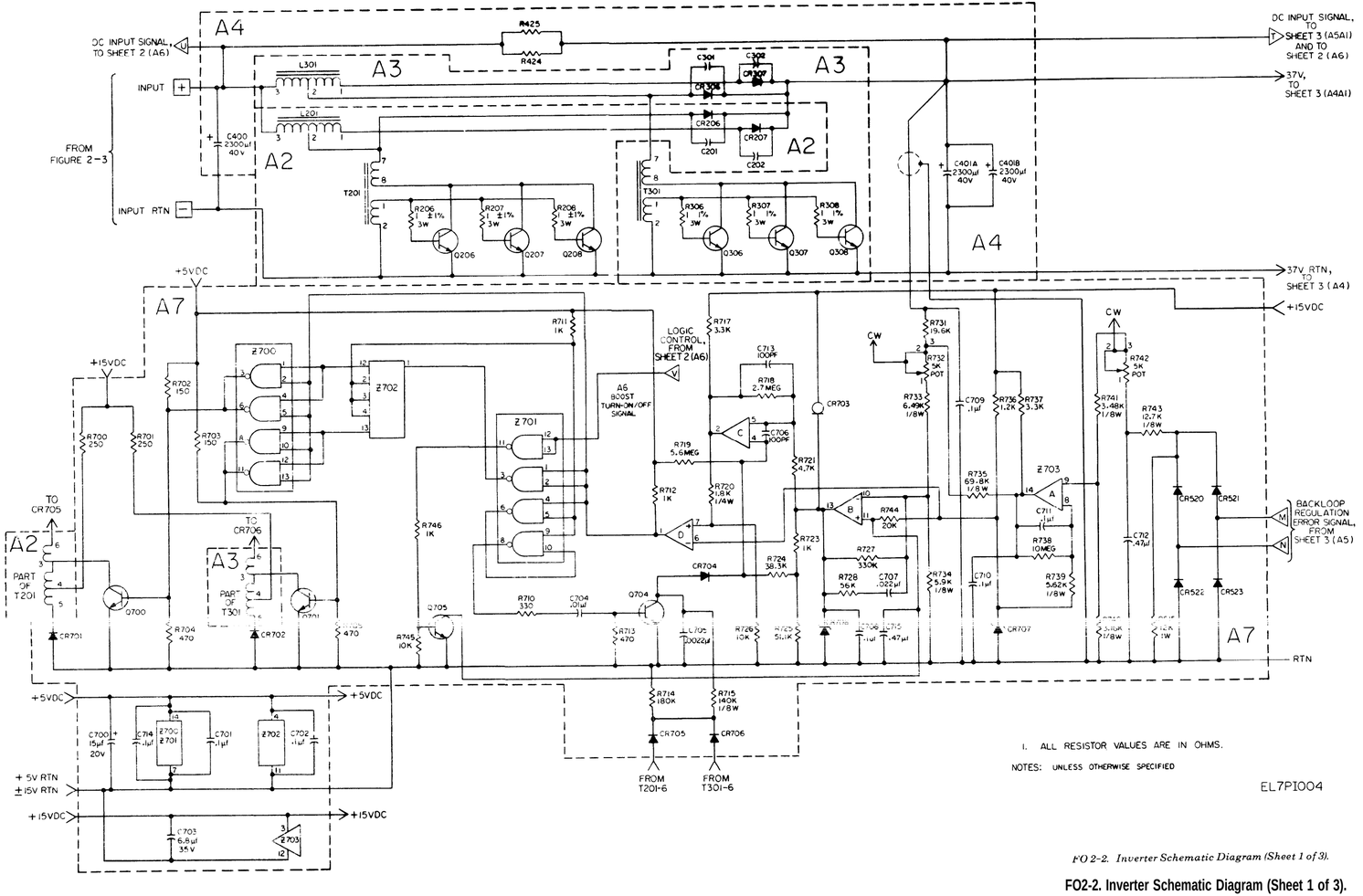
Perform tests delineated in paragraphs 3-5 and 3-6 to assure repaired inverter is completely Operational.

APPENDIX

REFERENCES

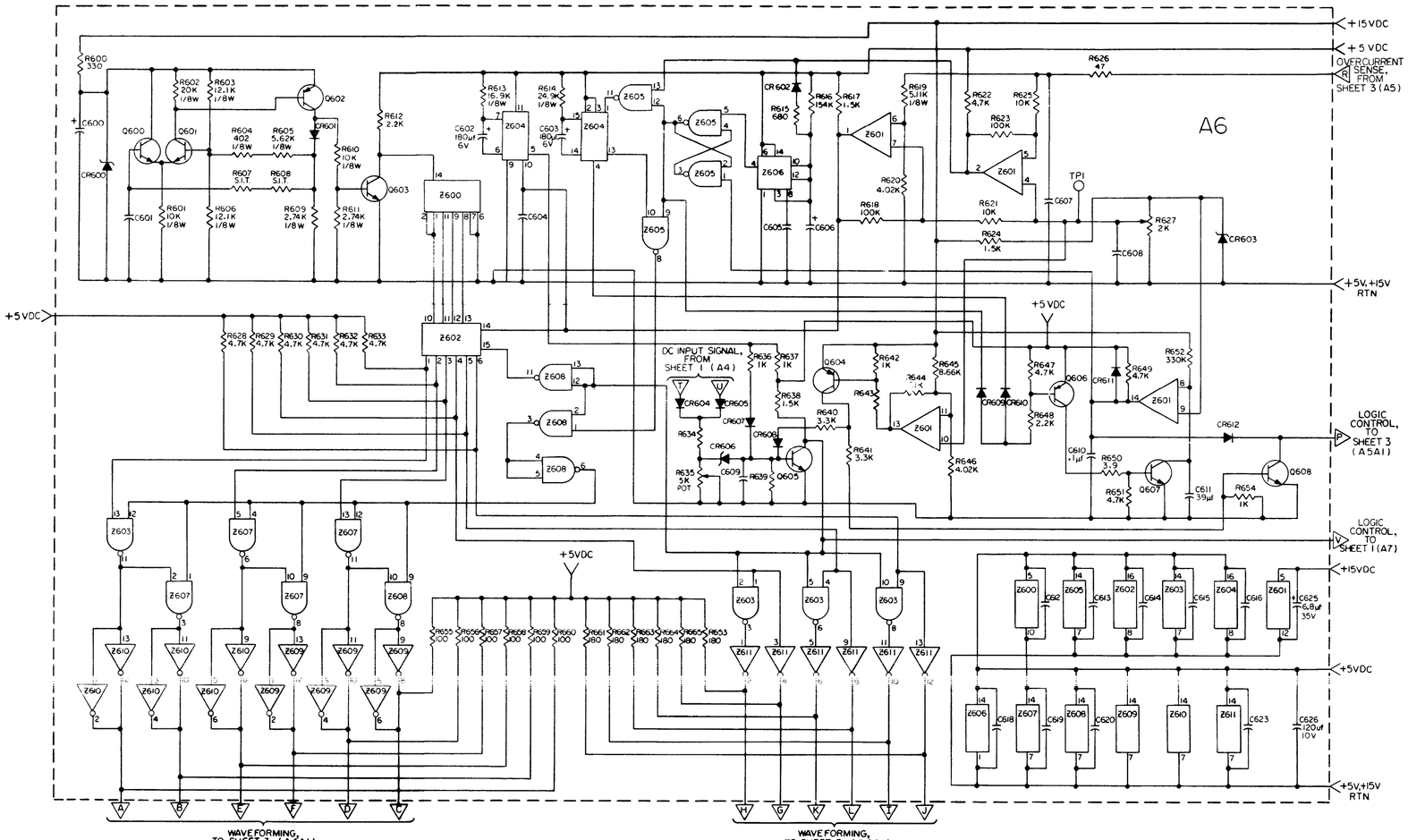
Following is a list of references applicable to direct and general support maintenance personnel of Static Power Inverter PP-7274C/A.

DA Pam 310-4	Index of Technical Publications.
SB 38-100	Preservation, Packaging and Packing Materials, Supplies, and Equipment used by the Army.
TM 11-1520-236-20	Organizational Maintenance Manual: Electronic Equipment Configurations, Army Model AH-lS Helicopter.
TM 11-6625-255-14	Operator's, Organizational, Direct Support and General Support Maintenance Manual: Spectrum Analyzer TS-723A/U, TS-723B/U, TS-723C/U, and TS-723D/U (NSN 6625-00-668-9418).
TM 11-6625-444-14-1	Operators, Organizational, Direct Support and General Support Maintenance Manual including Repair parts and Special Tools Lists: Voltmeter, Digital AN/GSM-64B (NSN 6625-00-022-7894) including Plug-In, Elecronic Test Equipment PL-1370/GSM-64B (NSN 6625-00-137-8366).
TM 11-6625-700-14-1	Operator, Organization, Direct Support and General Support Maintenance Manual Including Repair Parts and Special Tools List (Including Depot Repair Parts and Special Tools): Digital Readout Electronic Counter AN/KSM-207A (NSN 6625-00-044-3228).
TM 11-6625-2658-14	Operator's, Organizational, Direct Support and General Support Mainnance Manual for Oscilloscope AN/USM-281C (NSN 6625-00-106-9622).
TM 38-750	The Army Maintenance Management Systems (TAMMS)



FO 2-2. Inverter Schematic Diagram (Sheet 1 of 3).

FO2-2. Inverter Schematic Diagram (Sheet 1 of 3).



FO2-2. Inverter Schematic Diagram (Sheet 2 of 3)

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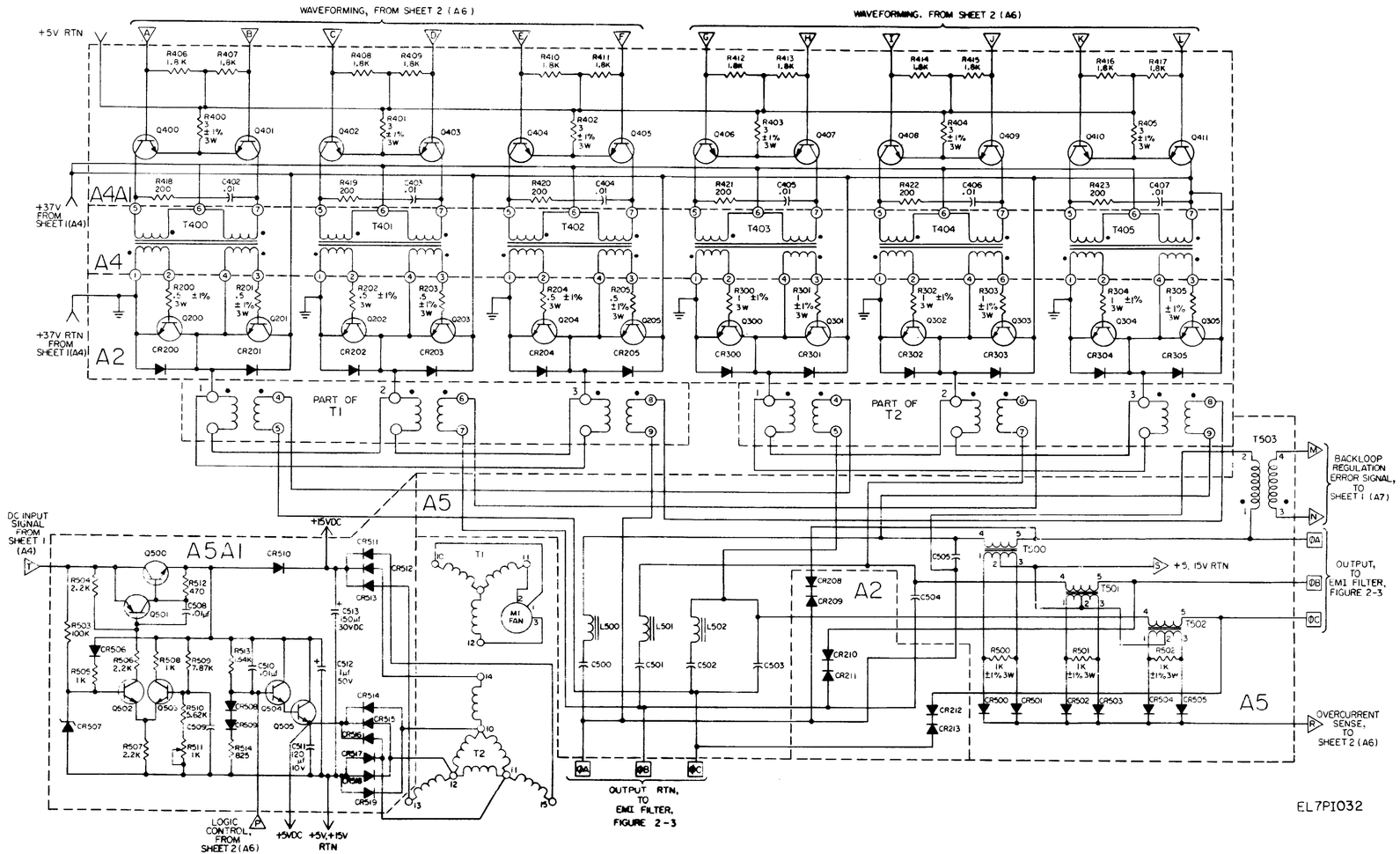
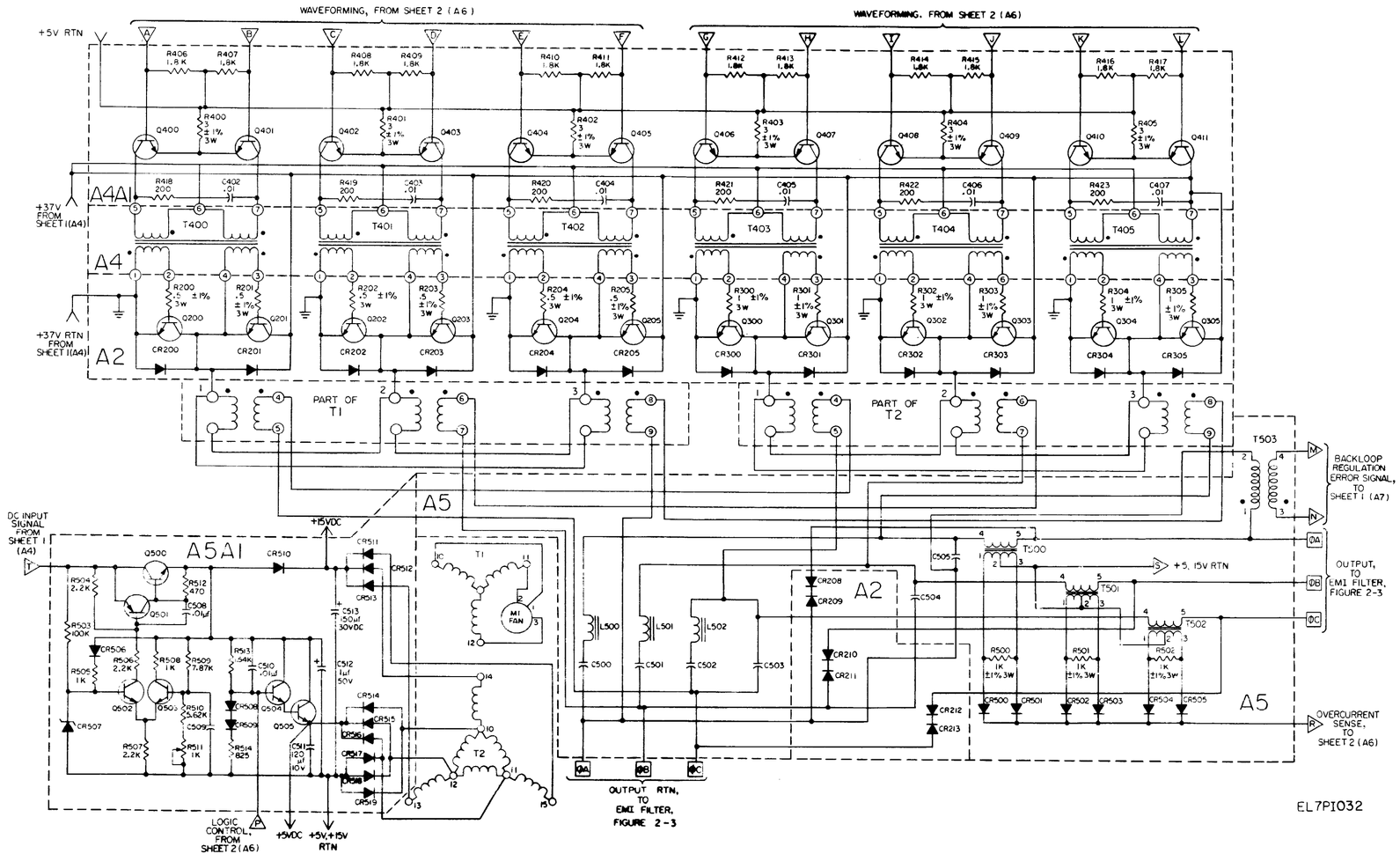
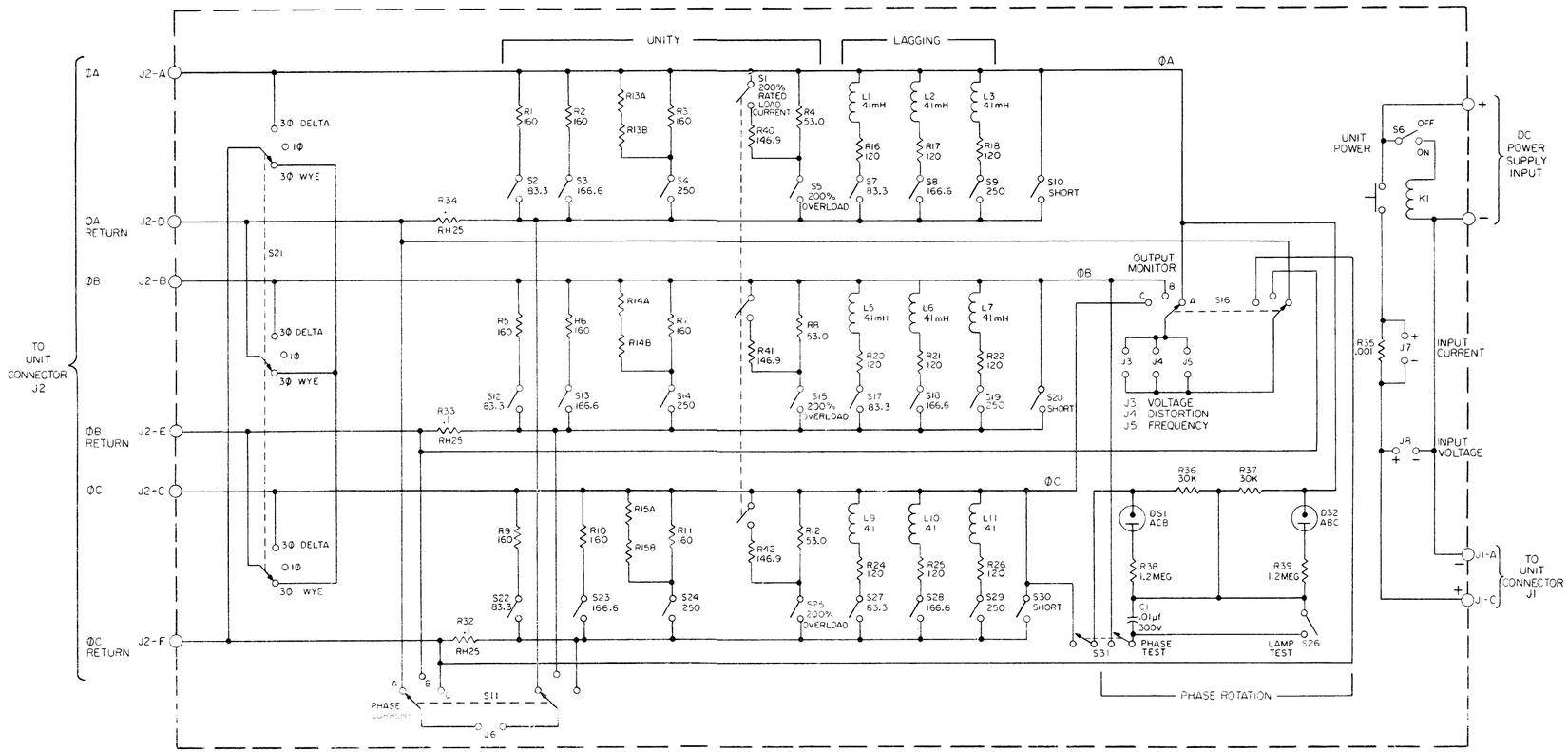


FO 2-2. Inverter Schematic Diagram (Sheet 3 of 3).

TM 11-6125-259-30



FO 2-2. Inverter Schematic Diagram (Sheet 3 of 3).



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS. ALL RESISTORS ARE RH100 AND ±1%.
2. VERIFY POWER FACTOR = .75 OR LESS. APPLY 400 Hz, 115V. MEASURE VOLTAGE ACROSS POWER RESISTORS (R16 ETC.) MEASURE VOLTAGE AMPS. $Pf = \frac{E^2/R}{VA}$
3. ALL CURRENT SHUNTS ±1%.
4. R13 A AND B, R14 A AND B, R15 A AND B, TRIM RESISTORS 3 WATTS.

EL7PI029

FO3-20. Test Fixture Schematic.

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DATE SENT: 10 July 1975

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

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PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure the the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

SAMPLE

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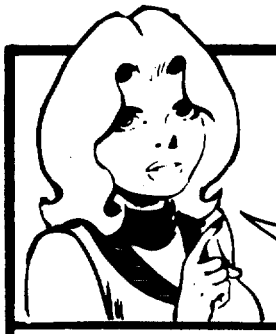

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